EVALUATION OF CERAMIC SUBSTRATES FOR PACKAGING OF LEADLESS CHIP CARRIERS

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AEH is performing extensive analysis and test work to develop analytical tools for predicting stress levels and thereby prevent failures in electronic assemblies composed of ceramics, metals and glass reinforced plastics when exposed to high level random vibration environments. The task is to determine a simple modeling procedure which will provide accurate results and which will be easy to verify during tests. The early work has been reported previously.[1] Although the reported results were acceptable, it was felt that limitations on the software routines being used were handicapping the accuracy of the results. The initial work used the SAPV2 software package which, (1) would not accept orthotropic materials properties, (2) would not accept damping as a function of frequency, and (3) would not calculate random responses. Subsequently, it was decided to adapt the model to MSC/NASTRAN to determine the extent to which the software handicaps influenced the results.

The Model:

The assembly being analyzed is composed of three high alumina ceramic substrates which are mounted to a glass reinforced multi-layer polyimide printed wiring board. The printed wiring board is mounted in a chassis by Wedge-Lok clamps which provide a rigid attachment at the two edges. The top edge and the bottom edge of the printed wiring board carry electrical connectors which serve to stiffen the edges on which they are mounted. Leadless chip carriers are soldered to both the printed wiring board and the ceramic substrates. The brass solder pins between the substrates and the printed wiring board provide both electrical and structural paths.

Figure 1 shows the assembly and how it was divided into plate and bar elements. Handbook values were used for mechanical properties of all the materials. The values used on MAT1 and MAT2 cards varied from handbook values as follows:

(1) The printed wiring board was stiffened to account for one ounce copper ground planes on both sides of the board.

(2) The printed wiring board density was increased to account for the copper ground plane as well as the thickness at a dipped solder coating on the ground planes.

(3) Both the printed wiring board and the substrate densities were increased to account for the mass of the leadless chip carriers and other electronic devices.

(4) The top and bottom connector shell densities were increased to account for a full complement of inserts and pins in each connector.

(5) The plates representing the substrate electrical pins were modeled as an orthotropic material with a low shear modulus compared to the Young's Modulus.

The non-structural mass feature of the properties cards was not used in order to preserve numerical similarity with the previous work. Neither was the composite capability of MSC/NASTRAN used to model the printed wiring board or the substrates. The only deviation from the previous SAPV2 model was the use of orthotropic plates to represent the substrate pins.

The Analysis:

The model was run in Solution 30, Modal Frequency Response, to determine the damping table which would closely duplicate the test accelerometer response. The first 20 modes were used and included all eigenvalues below 2,500 Hz. Structural damping is compared in Table 1. The Frequency Response Analysis showed a reasonably good agreement with the test data. Figure 2 compares the test data, the SAPV2 analysis and the MSC/NASTRAN analysis.

The model was then run in Solution 30, Random Response. The test accelerometer data was again fairly closely duplicated as shown in Figure 3. The goals of the modeling strategy were assumed to be achieved. The strains predicted by

MSC/NASTRAN model exposed to random excitation were then compared with the strain gauges on the test specimen.

Results:

Both the printed wiring board strains and the substrate strains were corrected slightly by the MSC/NASTRAN analysis using orthotropic plate elements to simulate the substrate pins. Table 2 compares the MSC/NASTRAN results with the SAPV2 calculations and the test strain gauges. Where SAPV2 was in error by a maximum factor of 2.94, MSC/NASTRAN was in error by a factor of 2.71. The use of orthotropic properties was not sufficient to fully correct the results of the finite element model.

Although the hoped for improvement in accuracy was not fully realized, two other side benefits of MSC/NASTRAN became evident:

(1) Twelve hours of hand calculations were required to convert SAPV2 Frequency Response data into Random Response data and were not necessary when using MSC/NASTRAN.

(2) Where it took four hours on an IBM 370 to solve the SAPV2 problem, it took only twelve minutes for MSC/NASTRAN on a Cyber 176 machine.

Conclusions:

Changing the model to orthotropic properties was insufficient to correlate the test data. Several other possible areas which may contribute sizable error are:

(1) Material non-linearity, particularly in the tin-lead solder which is quickly loaded beyond its elastic limit.

(2) Inaccurate materials properties. Handbook values for elastic properties of plastic and ceramics may be an error when the materials have been fabricated and modified for use in electronic packages. The composite materials capability of MSC/NASTRAN may correct some of this, but bending tests of "as fabricated" coupons may be necessary to accurately determine the elastic properties.

(3) Unrealistic distribution of damping by the modal superposition of real eigenvectors may be a problem. Solutions using complex eigenvalues or direct step-by-step integration may be able to correct it.

The above areas are being studied at AEH to correct the sources of the discrepancies. Until more reliable modeling strategies are developed, it should be assumed that the stresses and strains in ceramic substrates are significantly higher than finite element analysis predicts.

FOOTNOTE

(1) Analysis and Test of Ceramic Substrates for Packaging of Leadless Chip Carriers, A.E. Hatheway, and C. Montano, Institute of Environmental Sciences, March, 1982.

TABLE 1

STRUCTURAL DAMPING

SAPV2		MSC/NASTRAN	
f(hz.)	G	f(hz.)	G
100	.019	100	.044
560	.019	244	.044
560	.00864	487	.048
2000	.00864	1137	.019

TABLE 2

LOCAL STRAIN X 10^6

	.10 g^2/Hz			.40 g^2/Hz			1.6 g^2/Hz		
	SAPV2	MSC/N	Test	SAPV2	MSC/N	Test	SAPV2	MSC/N	Test
PWB Front	99.0	79.5	68.2	197.9	15.9	85.2	395.8	318.	187.5
Substrate #1a	13.7	14.9	33.9	27.4	29.7	76.3	54.7	59.4	161.1
Substrate #1b	11.7	12.3	25.6	23.4	24.7	59.7	46.8	49.4	110.8
Substrate #2		15.3	Survive		30.6	Surv.		61.3	Fract
Substrate #3		25.5	Survive		51.0	Surv.		102.	Fract

FIGURE I

LEADLESS CHIP CARRIER ASSEMBLY

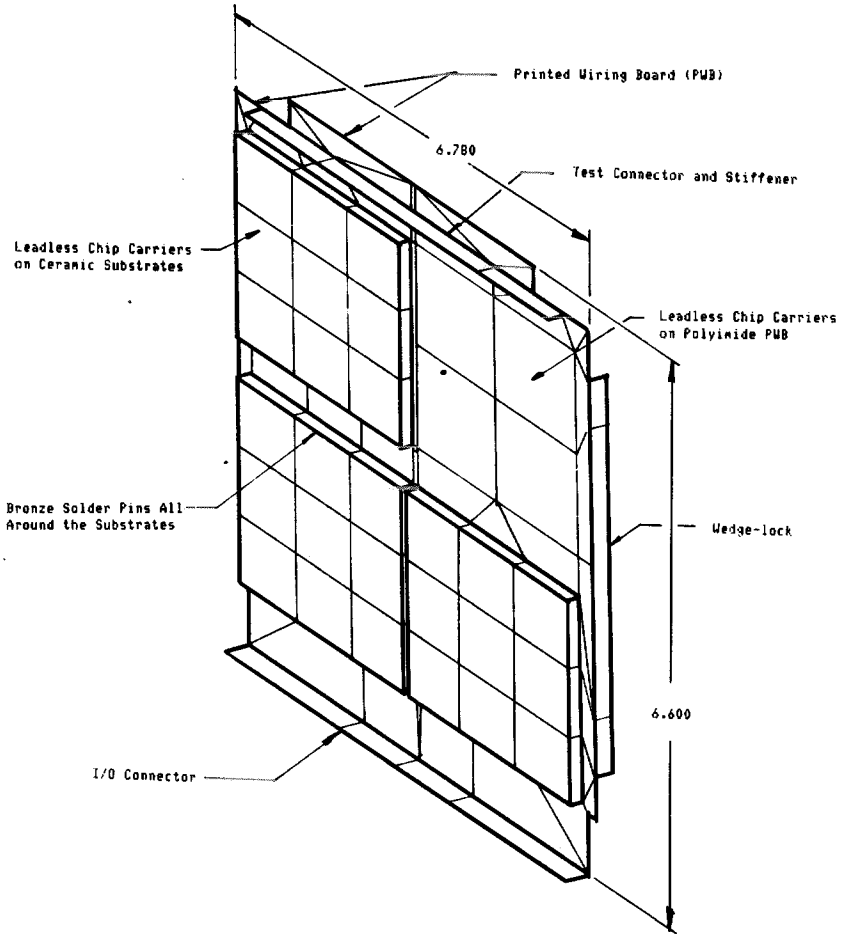

FIGURE 2

FREQUENCY RESPONSE COMPARISON, 5G INPUT

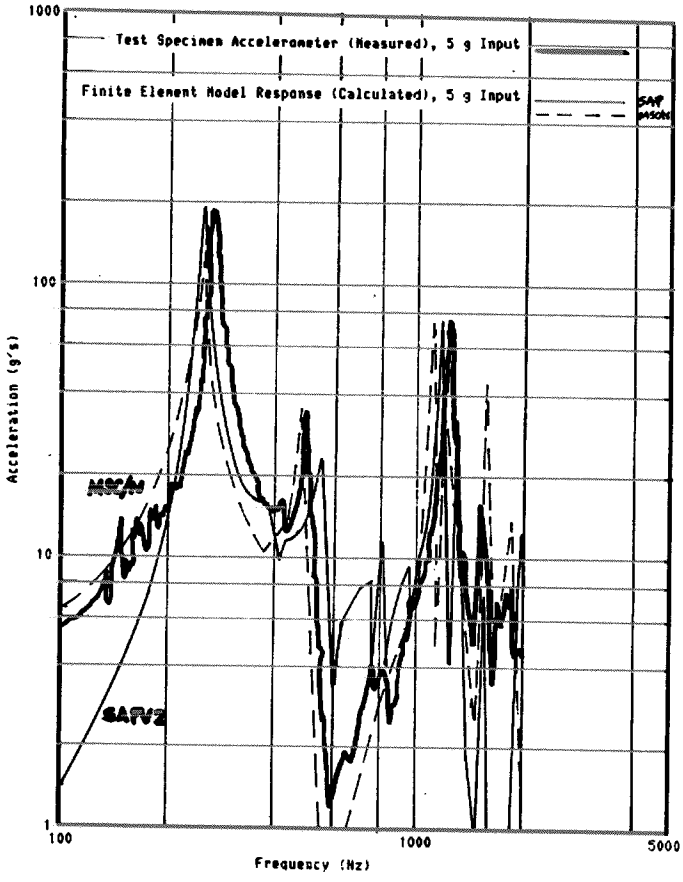

FIGURE 3

RANDOM RESPONSE COMPARISON, .40G SQUARED/HZ. INPUT