FINITE ELEMENT THERMAL ANALYSIS OF DARLINGTON TRANSISTOR STACK

by

John R. Cotner
Barbara A. McCann

Electronic Technology Development
and Components Engineering Department

Electrical and Electronics Division
Product Engineering Office

Ford Motor Company

Presented at
MSC/NASTRAN USERS' CONFERENCE

March 22-23, 1984

Pasadena, California

ABSTRACT

The results of a three-dimensional, steady state finite element thermal analysis of a transistor stack consisting of a power darlington transistor, solder, a beryllium oxide heat spreader and an aluminum base plate are presented. The temperature rise of the transistor, which contains the heat generation source, predicted by the model is within 4% of the temperature rise measured in the laboratory. The model can be used as a basis for evaluating the thermal effects of alternate constructions of heat sinks and of variations in solder wetting.

INTRODUCTION

Thick film hybrid circuits are finding wider application in the automotive industry in recent years. An important use of this technology is found in the Thick Film Ignition (TFI) module, part of the Electronic Engine Control System on Ford engines. The TFI module provides more efficient engine operation by controlling the amount of energy that is released to the ignition coil. Previously, a constant amount of energy was delivered to create the spark; now the TFI module controls the amount of energy delivered which depends on a signal from the distributor.

The ignition coil is driven by a power darlington transistor within the TFI module. The darlington often generates an excessive amount of heat due to the combination of high battery

voltage, high current and long dwell time, which occurs under certain engine conditions. If this generated heat is not properly dissipated away from the darlington transistor, the device will go into a condition known as thermal runaway at about 200°C.

The main controlling device for the TFI module is its integrated circuit. This is sychronized with the distributor output via the Electronic Engine Control module, and controls the charging and dwell times for the coil based on engine operating conditions. The coil charging occurs in a ramp-like fashion as illustrated in Figure 1, a plot of the current in the darlington transistor versus time.

The ramp up, dwell time, and energy dissipation times vary being controlled by engine RPM and the engine operating condition. In the START MODE, the coil remains charged for a long period of time (50% of the duty cycle) to insure a high energy spark for engine start up. Although the darlington transistor experiences a high current input for a large percent of the duty cycle during this condition, the temperature rise is not a concern since the module is in the START MODE for a very short period of time.

Under normal engine operation the module is in the RUN MODE. During this time the dwell can vary from 20 to 30% of the duty cycle according to engine RPM. An analysis of the worst case condition (idle at 750 RPM and 30% dwell time) was completed along with other darlington transistor loading conditions which were used to verify the model.

The purpose of the work described below was to begin to develop a base for analyzing the thermal properties of electronic products for automobiles by employing techniques using the finite element method. So it was considered important that the more expensive (in terms of computer resources) capabilities of MSC/NASTRAN, e.g., non-linearities and/or super elements, not be used. As will be shown below, static thermal analysis (MSC/NASTRAN solution sequence 24) produced excellent results. The thermal analysis was conducted on the darlington transistor stack which consists of the darlington transistor, a beryllium oxide (BeO) heat spreader, an aluminum (Al) heat sink and two solder layers: one between the transistor and the beryllium oxide and the other between the beryllium oxide and the aluminum. The transistor is made of silicon (Si).

FINITE ELEMENT MODEL

The model was made by using MSGMESH (1)* because of the regular pattern of 8-noded CHEXA (rectangular parallelpipeds) elements that could be used to approximate the darlington transistor stack and the small dimension of the parts in the stack. Since MSGMESH produces grid point numbers that span a wide range (because they are based upon field numbers), a DMAP (Direct Matrix Abstraction Programming) alter, RF24D74, (2) was used to approximately halve the computer solution time on a CYBER 176. The purpose of this change to the DMAP solution sequence number 24 was to provide for the internal

---

* Numbers in parenthesis denote the references listed at the end of the paper.

resequencing of geometric grid points and scalar points in order to improve the efficiency of decomposition and equation solution operations.

The aluminum base plate which attaches to the distributor (in the automobile's engine compartment) is 26.1 mm wide (X-direction), 19.8 mm deep (Y-direction) and 1.6 mm thick (Z-direction). The beryllium oxide heat spreader is 11.7 mm wide, 8.1 mm deep and 0.64 mm thick. The transistor is 5.4 mm wide, 6.3 mm deep and 0.3 mm thick. The small size of the elements was dictated by the thickness of the solder layers. Without the inclusion of the solder layers in the model the difference between the temperature rise of the beryllium oxide and that of the transistor could not be as accurately calculated.

The elements were 0.9 mm in both the X and Y directions. Where possible the aluminum elements were made 1.8 mm in the X and Y directions. Figure 2 shows the X-Z plane of the model. A perspective view is shown in Figure 3. The solder layers cannot be resolved in either one of these figures. Figure 4 shows the X-Z plane of the model with the Z dimensions expanded 10 times. The two solder layers can be seen in this figure. Figure 5 is a perspective view of the model with the Z dimensions expanded 10 times.

To model the conduction of the generated heat away from the transistor AREA4 CHBDY's (3) were put on the bottom of

the aluminum (Z=0 plane). A heat conducting surface was not put on the top of any of the components in the transistor stack since the worst case for heat dissipation from the transistor was being modeled. Also since the aluminum heat sink is fixed to the distributor, no heat loss due to radiation was modeled.

After the darlington transistor stack and the other electronic components in the TFI module are assembled, an 8 mm thick layer of Dow Corning 3-6527 silicon dielectric gel (sil gel) is poured into the module's case and cured. The sil gel is added to protect the electronic components from excessive moisture. Inclusion of the sil gel in the thermal model results in a cooling of the transistor of 0.46°C/watt-sec. at the location of its maximum temperature rise. Since a worst case thermal calculation was desired, the sil gel was not included in the model the results of which are reported below.

DESCRIPTION OF THE THERMAL EXPERIMENT

The transistor stack, Figure 6, was mounted on a hot plate, Figure 7, which served as a heat sink. No sil gel was put on the components in the transistor stack, but solder was in between the transistor and the beryllium oxide and between the beryllium oxide and the aluminum. Thermocouples were connected as shown in Figure 7. Energy was applied to the transistor as shown in Figure 1 with the duty cycle set at 20Hz (50 ms/cycle). The rise time from zero to 6.5 amps

was 4 milliseconds (8% of the duty cycle). During the rise time the voltage was 1.5 volts. So for all settings of the dwell time 0.39 watt-sec. was put into the transistor during the rise time. The calculation of the energy put into the emitter is contained in the Appendix. During the dwell time the voltage varied from 10.0 volts at 10% dwell to 9.7 volts at 50% dwell. The energy was 6.9 watt-sec. at 10% dwell going up to 31.9 watt-sec. at 50% dwell. Table I contains the experimental results compared to the results from the finite element model.

FINITE ELEMENT MODEL RESULTS

The comparison of the temperature rise predicted by the finite element model which is shown in Table I was for points in the model corresponding to the placement of the thermocouples in the laboratory experiment. These points on the transistor, beryllium oxide and aluminum were chosen so that the results of the model could be verified by experimental measurements. They are not the points in which the highest temperature rise per watt-sec. occurred in the analytical results. The points with the greatest temperature rise are in the middle of the emitter of the transistor (the heat generator) and directly below the middle of the emitter for the beryllium oxide and the aluminum. These points are on or under the center of the line labeled 70°C in the temperature contour plot that is in Figure 8. This plot is the result of a thermal analysis of the transistor stack with

the bottom of the aluminum held at 24°C with 19.7 watt-sec. put into the emitter. This is the same as the laboratory experiment done at 30% dwell. These highest temperature rises are shown in Table II. Figures 9 through 12 contain temperature contours of just the transistor that are the result of this same analysis. In Figures 9 and 10 are views of the top and sides of the transistor with temperature contours. Figure 11 contains a side view of the transistor, while Figure 12 contains the temperature contours on the bottom of the transistor.

At 30% dwell time with the TFI in RUN MODE (engine idling at 25 Hz) the amount of thermal energy in the emitter is slightly less than 20 watt-sec. From the data in Table II it can be seen that the transistor will not reach 200°C (the temperature at which thermal runaway occurs) even if the temperature of the distributor rises to 140°C. Therefore the analysis shows that even in the worst case the darlington transistor will not reach thermal runaway.

As stated above, it was necessary to include the solder in the model to more accurately predict the difference in the temperature rise between the transistor and the beryllium oxide. From data in Table I it can be seen that the difference in the temperature rise between the transistor and the beryllium oxide is 0.39°C/watt-sec. If the solder is not included in the model, this difference is 0.20°C/watt-sec. The temperature of the beryllium oxide falls more than that

of the transistor when the solder is included in the model since the solder is on both sides of the beryllium oxide and only on one side of the transistor. That is, the inclusion of the solder cools the beryllium oxide more than it cools the transistor.

CONCLUSION

It can be concluded from this study that three-dimensional thermal analyses using the finite element method can be employed to accurately predict the thermal properties of electronic products with internal heating. The model used in this study can also be used to evaluate alternate constructions of heat sinks for electronic products and variations in solder wetting. Models using the same technology can be used to determine the thermal reaction of other electronic products, e.g., the heating of thick films due to the heat generated in resistors and integrated circuits.

APPENDIX

The energy expended in the transistor during the laboratory experiment at 30% dwell will be developed. Figure 13 contains a plot of two 20 Hz cycles of the power versus time. During the rise of the emitter current in the darlington transistor from 0 to 6.5 amps in 4 milliseconds of a 20 Hz cycle (50 msec. cycle time), the voltage was 1.5 volts. The amperage rise is almost linear (the assumption made in Figure 13). So the energy is:

$$(1/2) * (4/50) * (6.5) * (1.5) = 0.39 \text{ watt-sec.}$$

During the dwell time the power is:

6.5 amps * 9.9 volts = 64.35 watts

The total energy is:

0.39 + (30% dwell) * 64.35 = 17.9 watt-sec.

REFERENCES

1. Peterson, Leonard, Editor, "MSGMESH Analyst's Guide," The MacNeal-Schwendler Corporation, Los Angeles, CA. April, 1978 (revised December, 1982)

2. McCormick, Caleb W., Editor, "MSC/NASTRAN User's Manual Version 62, Section 3.5". The MacNeal-Schwendler Corporation, Los Angeles, CA May 1976 (revised Feb. 1981)

3. _Ibid_, Section 2.4

TABLE I

RESULTS OF THERMAL EXPERIMENT AND OF THE FINITE ELEMENT MODEL

	Average °C/Watt-sec. for 10 to 50% Dwell Time		
	Transistor	Beryllium Oxide	Aluminum
Experimental Results	1.71	1.32	1.00
Finite Element Model Results	1.68	1.29	0.91
Percentage Difference	2	2	9

Average difference 4 percent

TABLE II

MAXIMUM TEMPERATURE RISE IN TERMS OF THERMAL ENERGY

	Degree Centigrade per Watt-sec.		
	Transistor	Beryllium Oxide	Aluminum
Finite Element Model Results	2.73	2.41	2.07

FIGURE 1

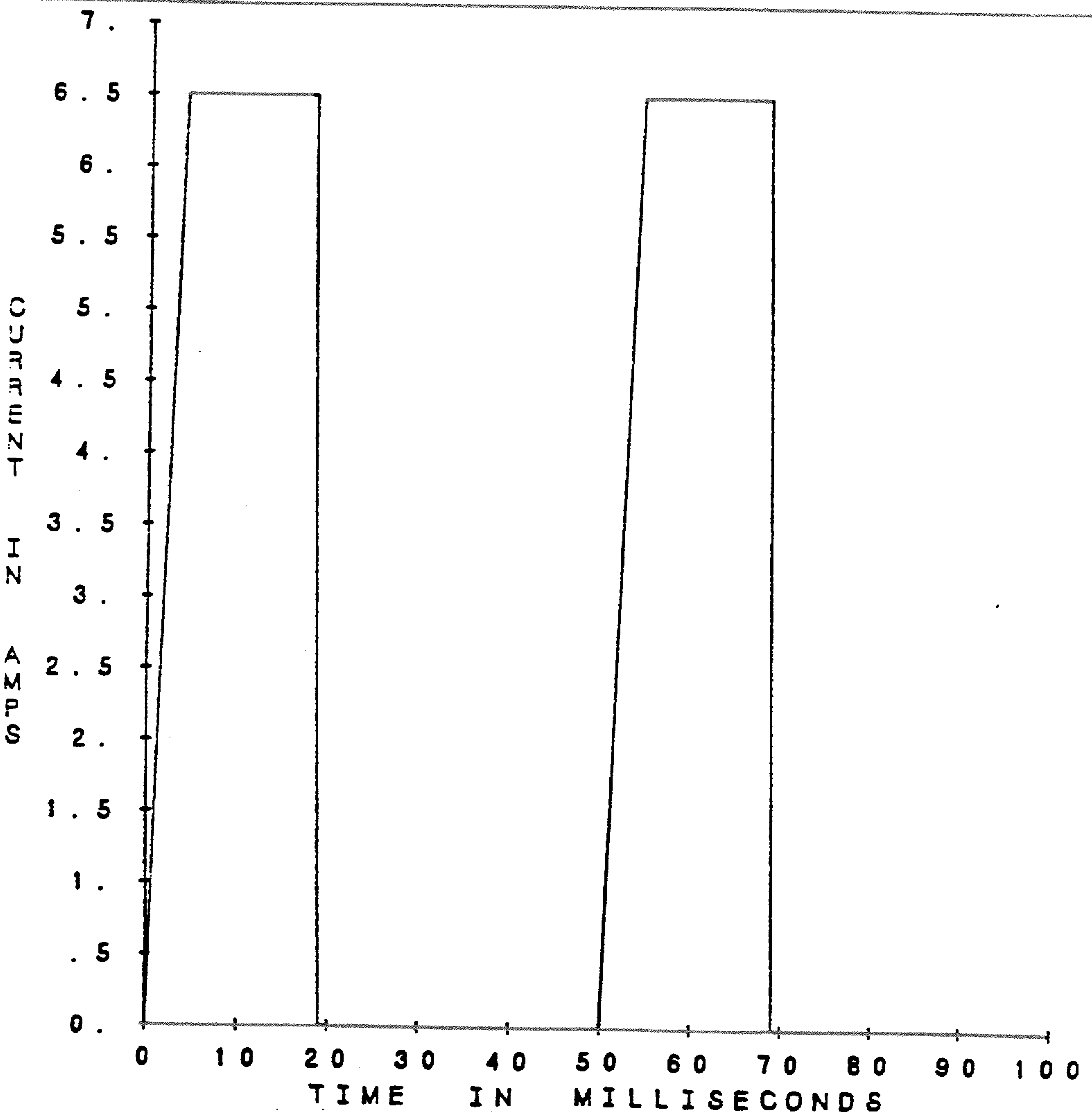


FIGURE 2

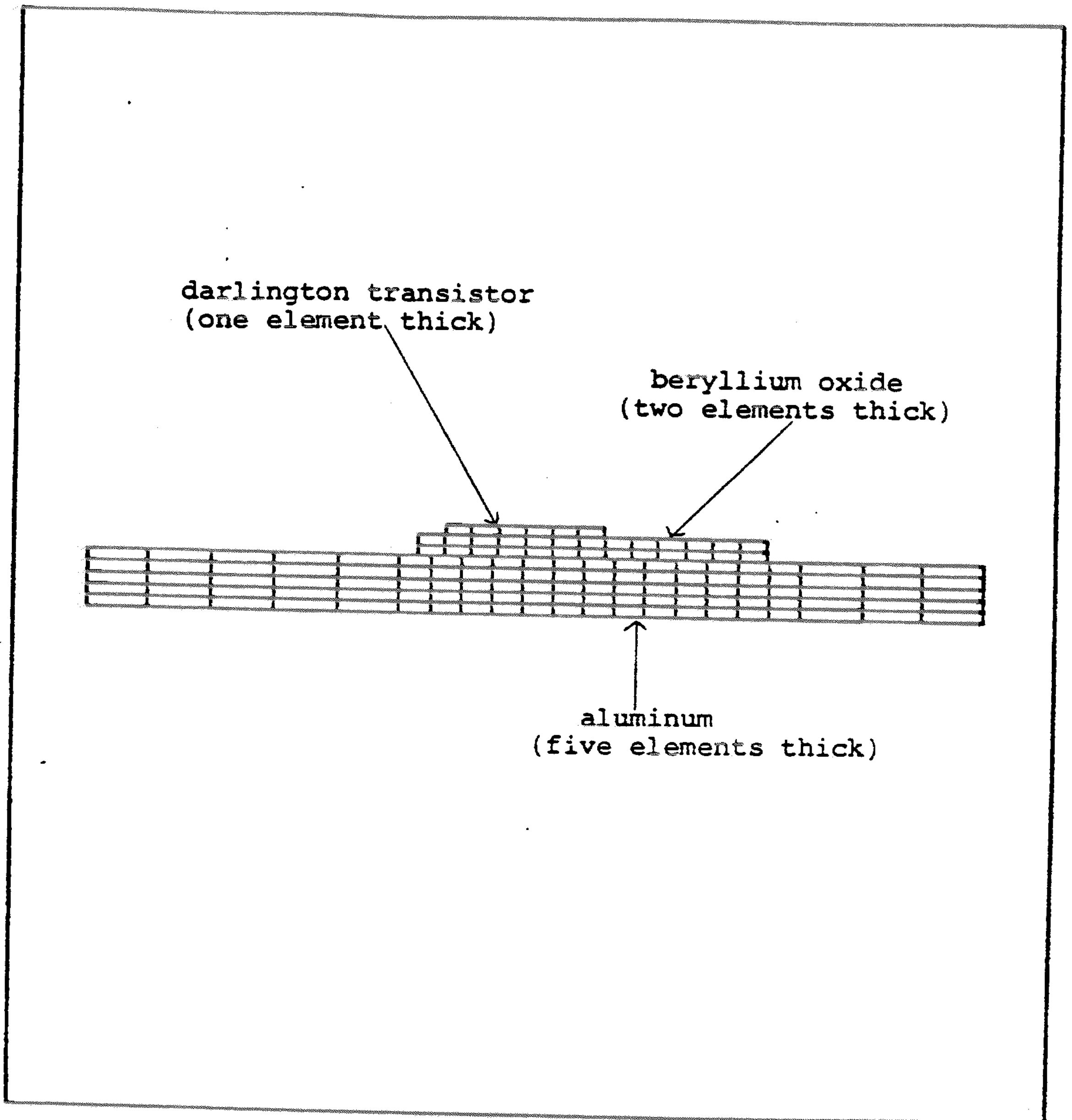


FIGURE 3

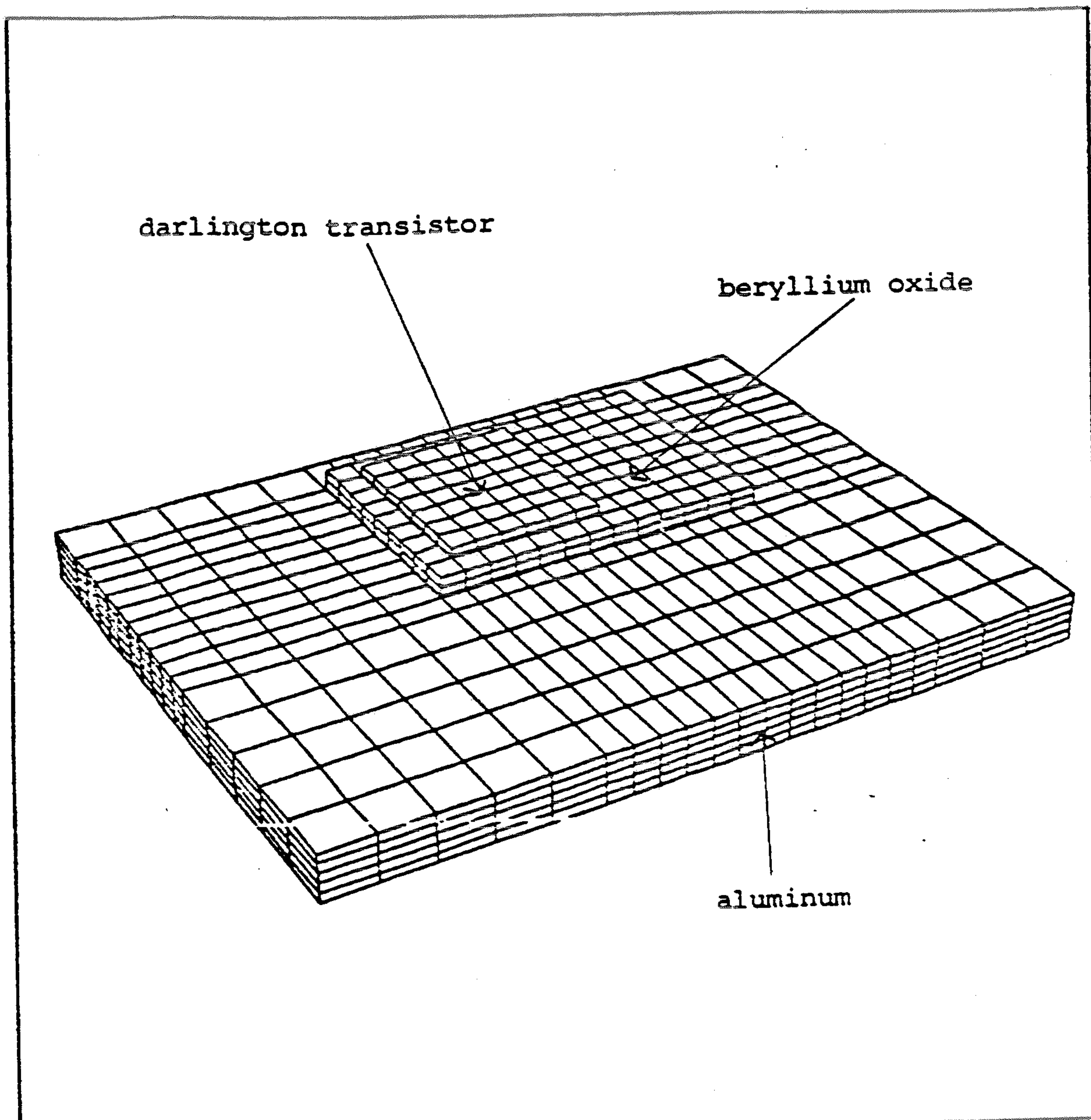


FIGURE 4

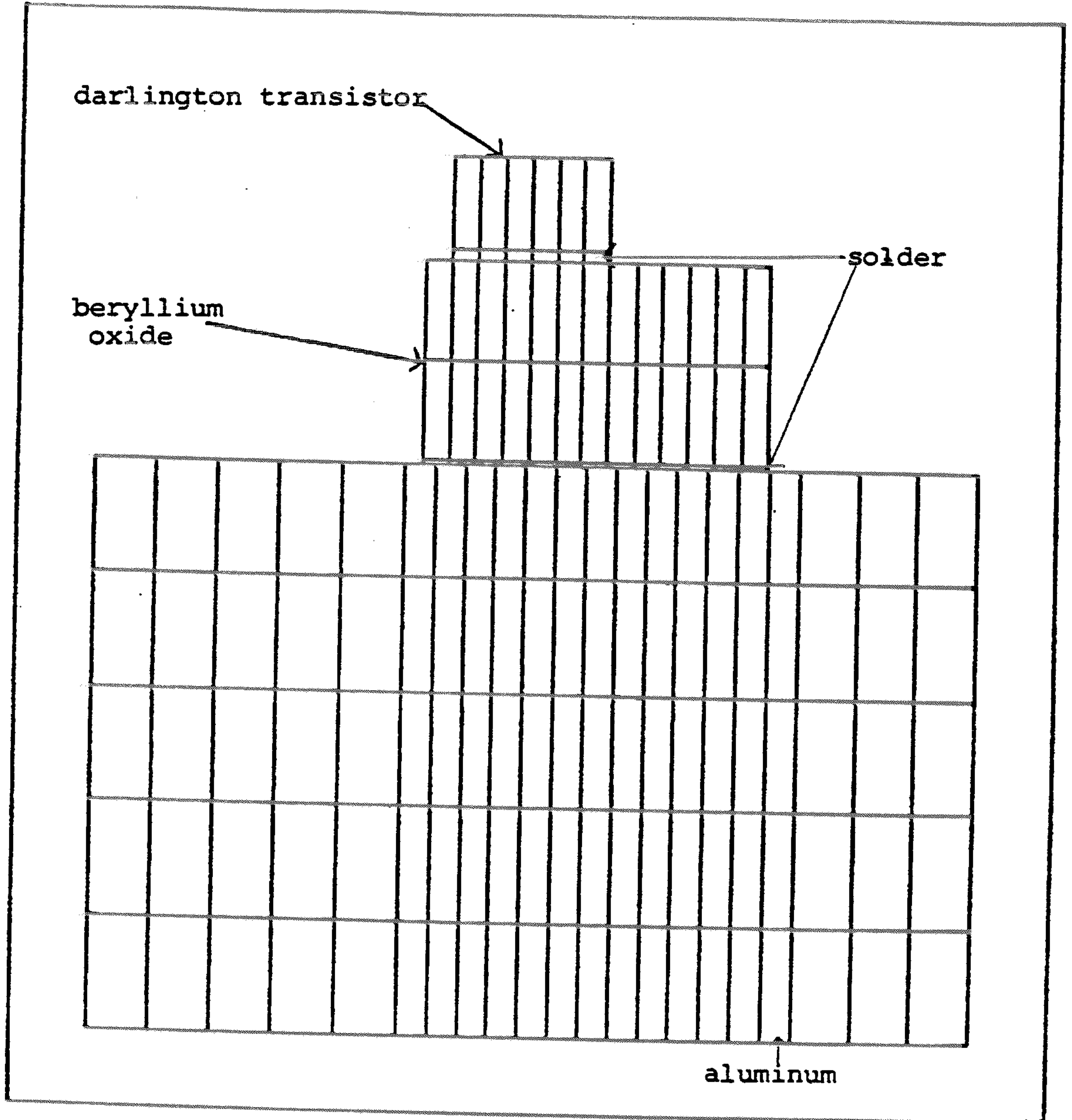


FIGURE 5

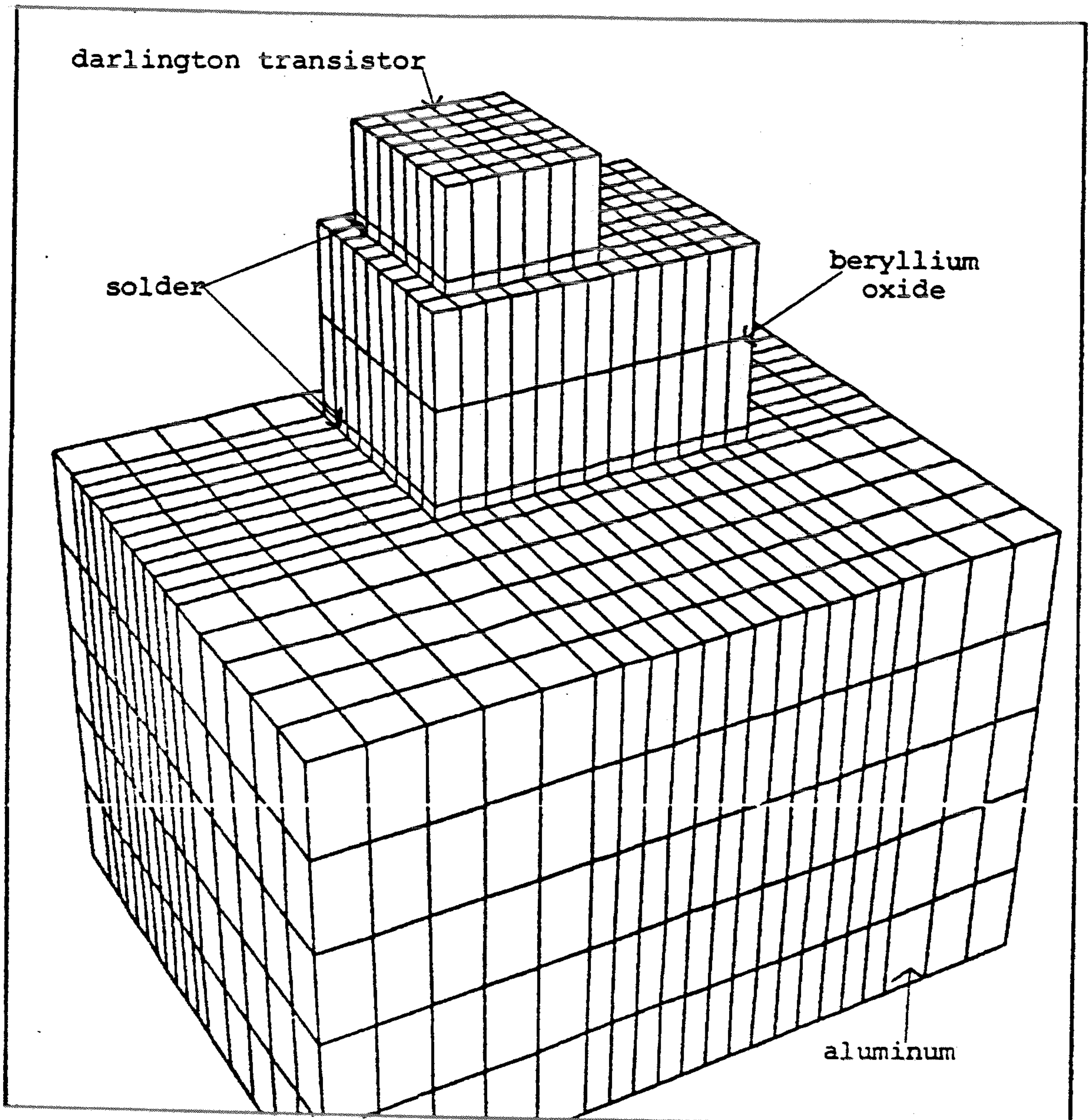
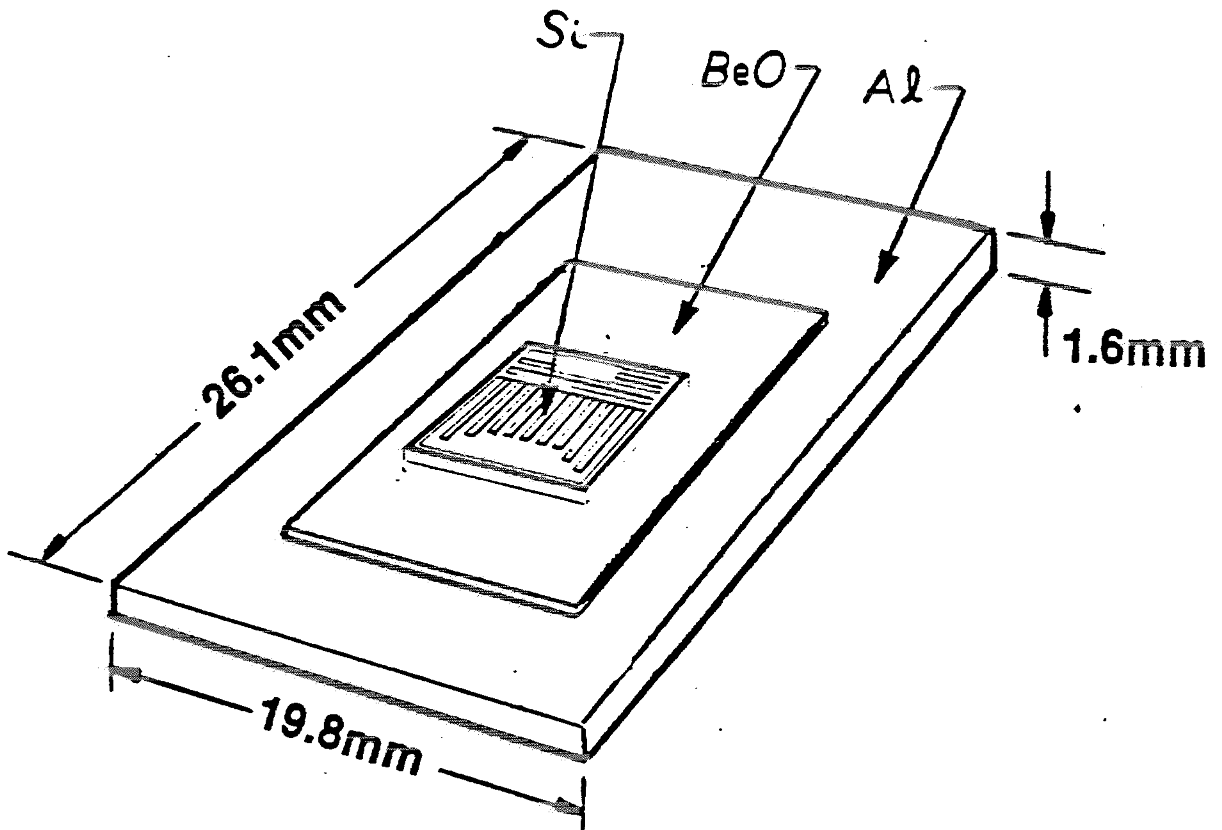
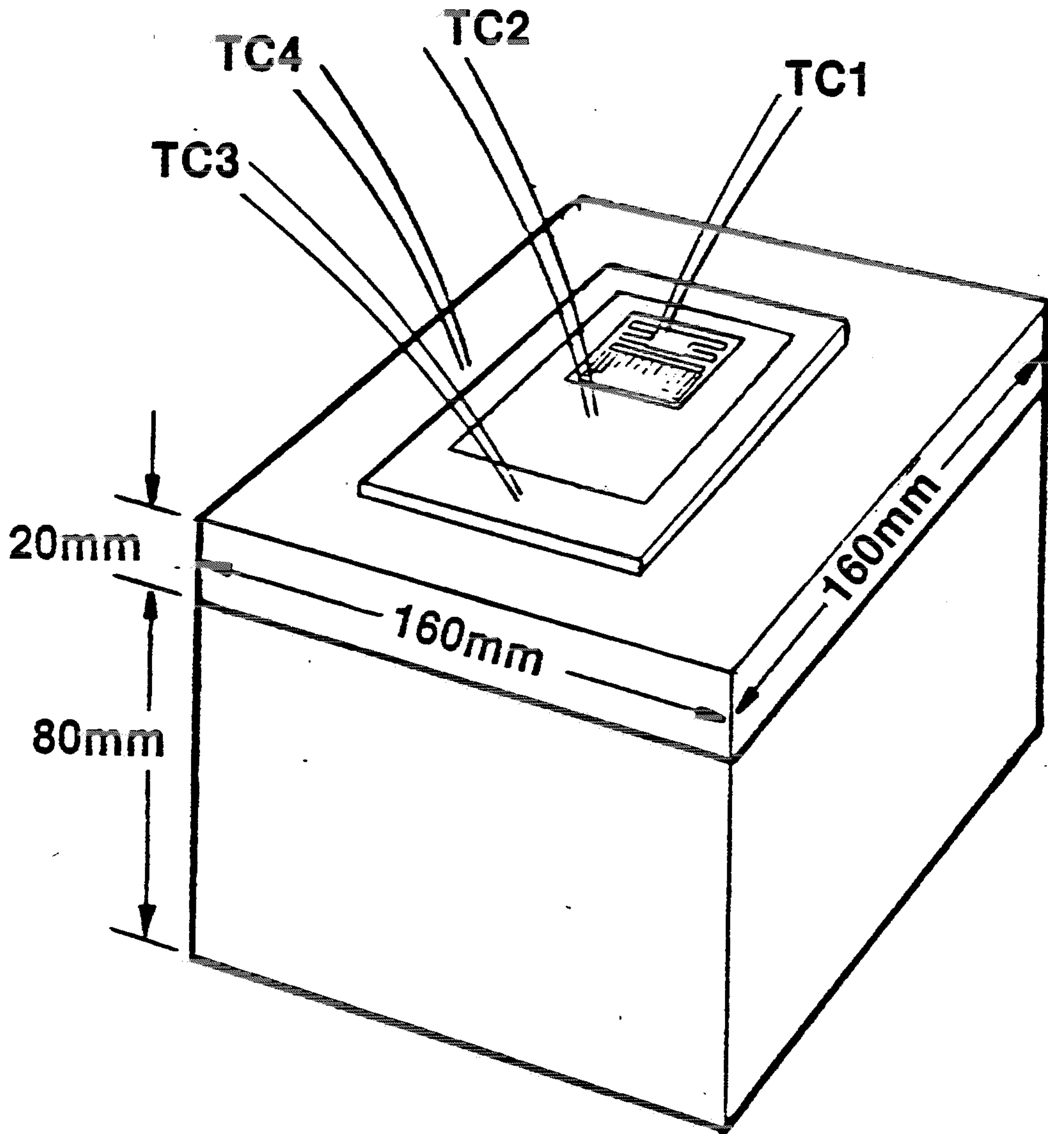


FIGURE 6



DARLINGTON TRANSISTOR STACK

FIGURE 7



HOT PLATE USED AS HEAT SINK FOR DARLINGTON TRANSISTOR STACK THERMAL EXPERIMENT

FIGURE 8

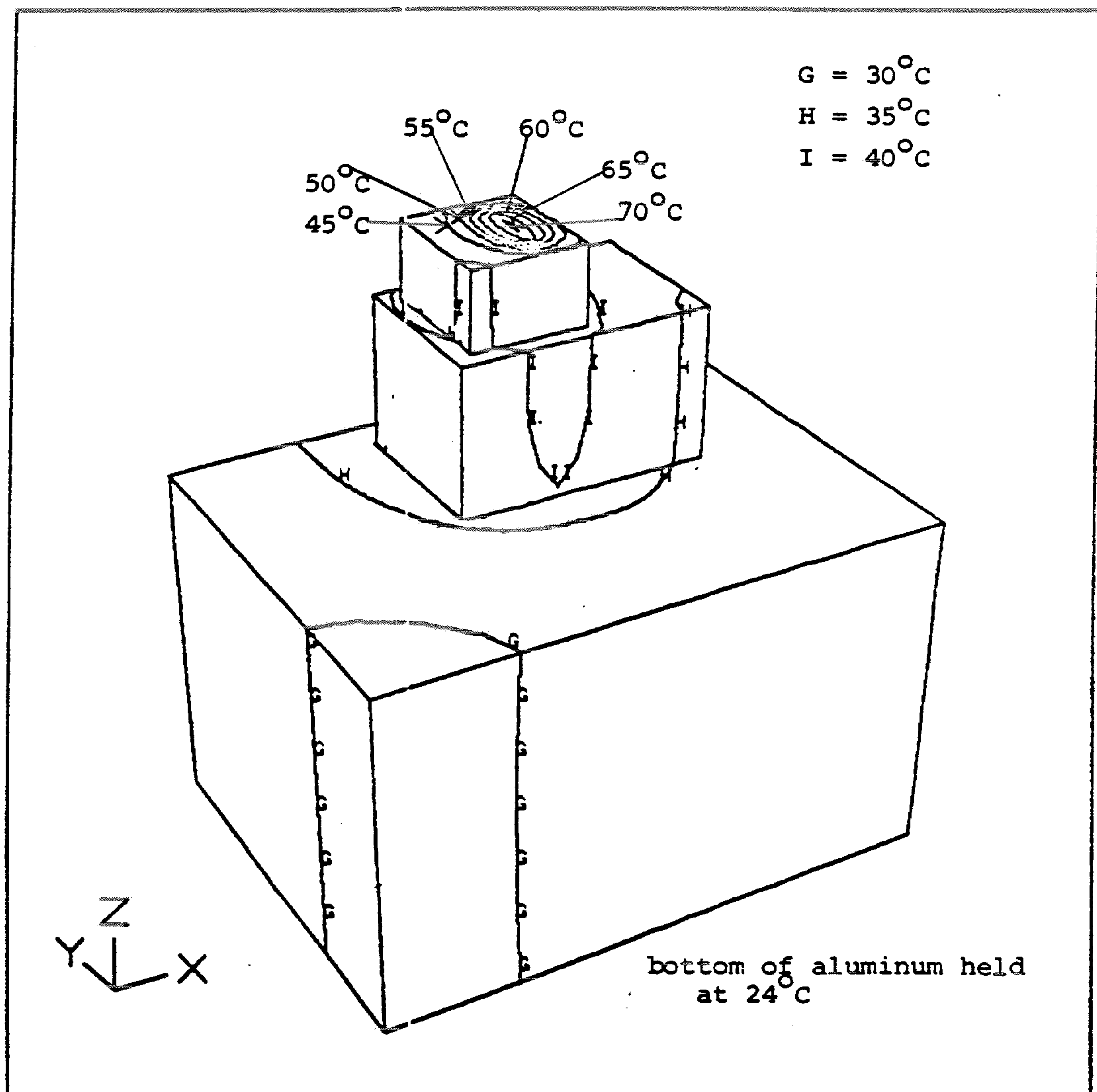


FIGURE 9

I = 40°C
J = 45°C
K = 50°C
L = 55°C
M = 60°C
N = 65°C
O = 70°C

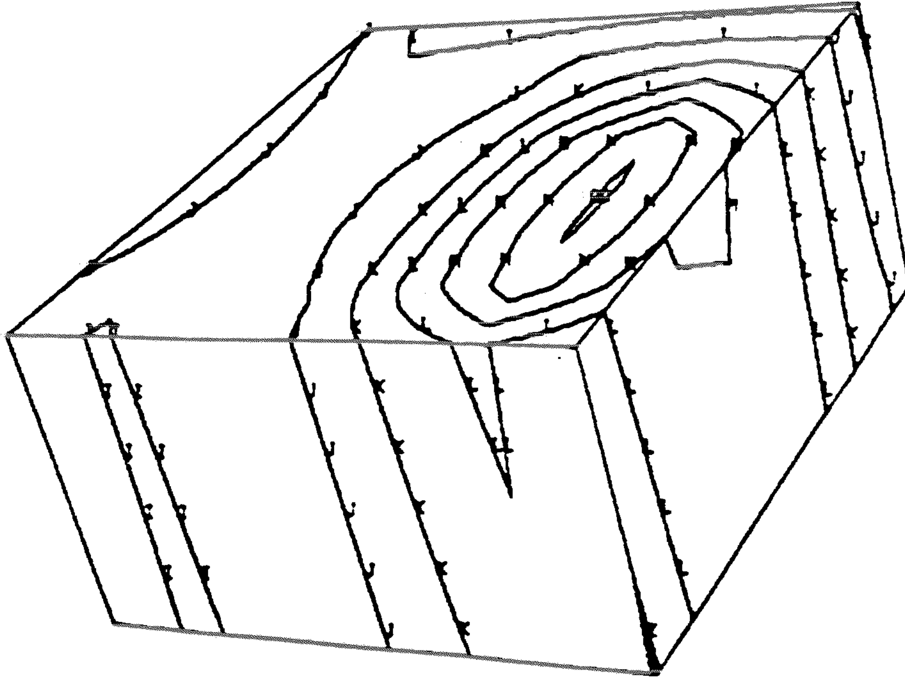


FIGURE 10

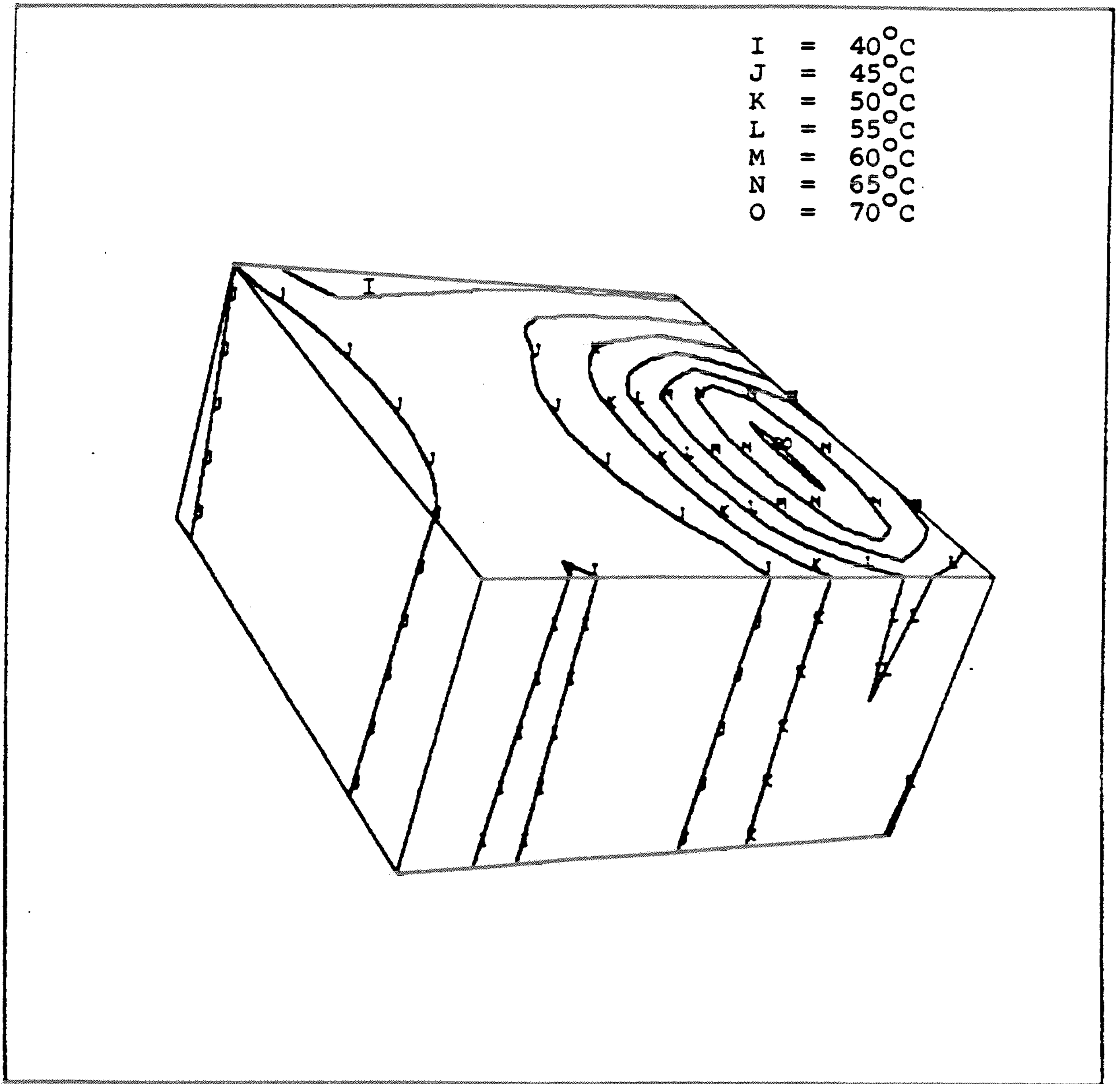


FIGURE 11

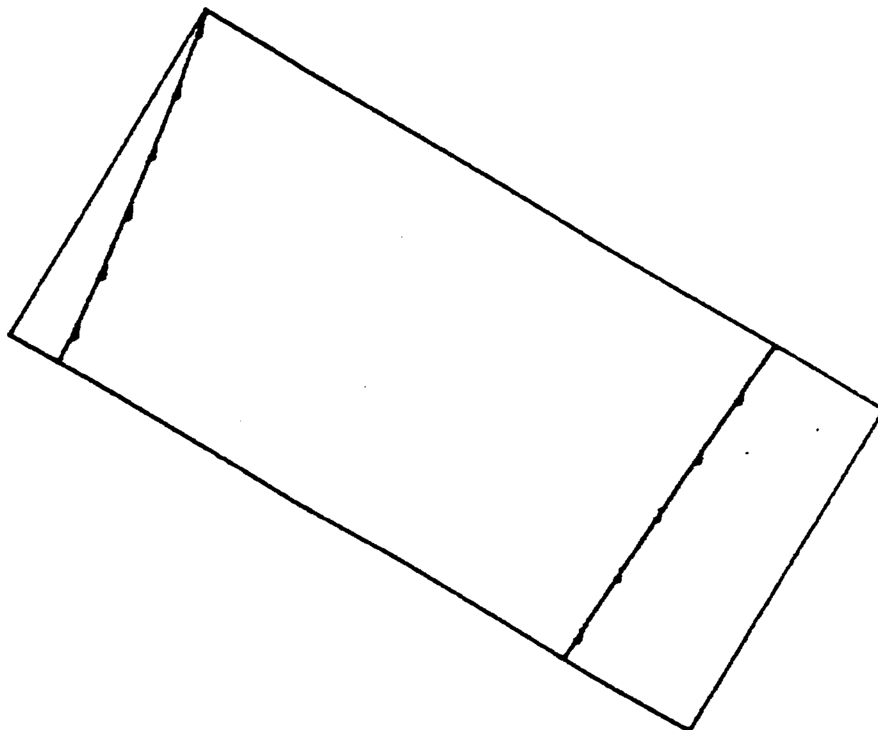


FIGURE 12

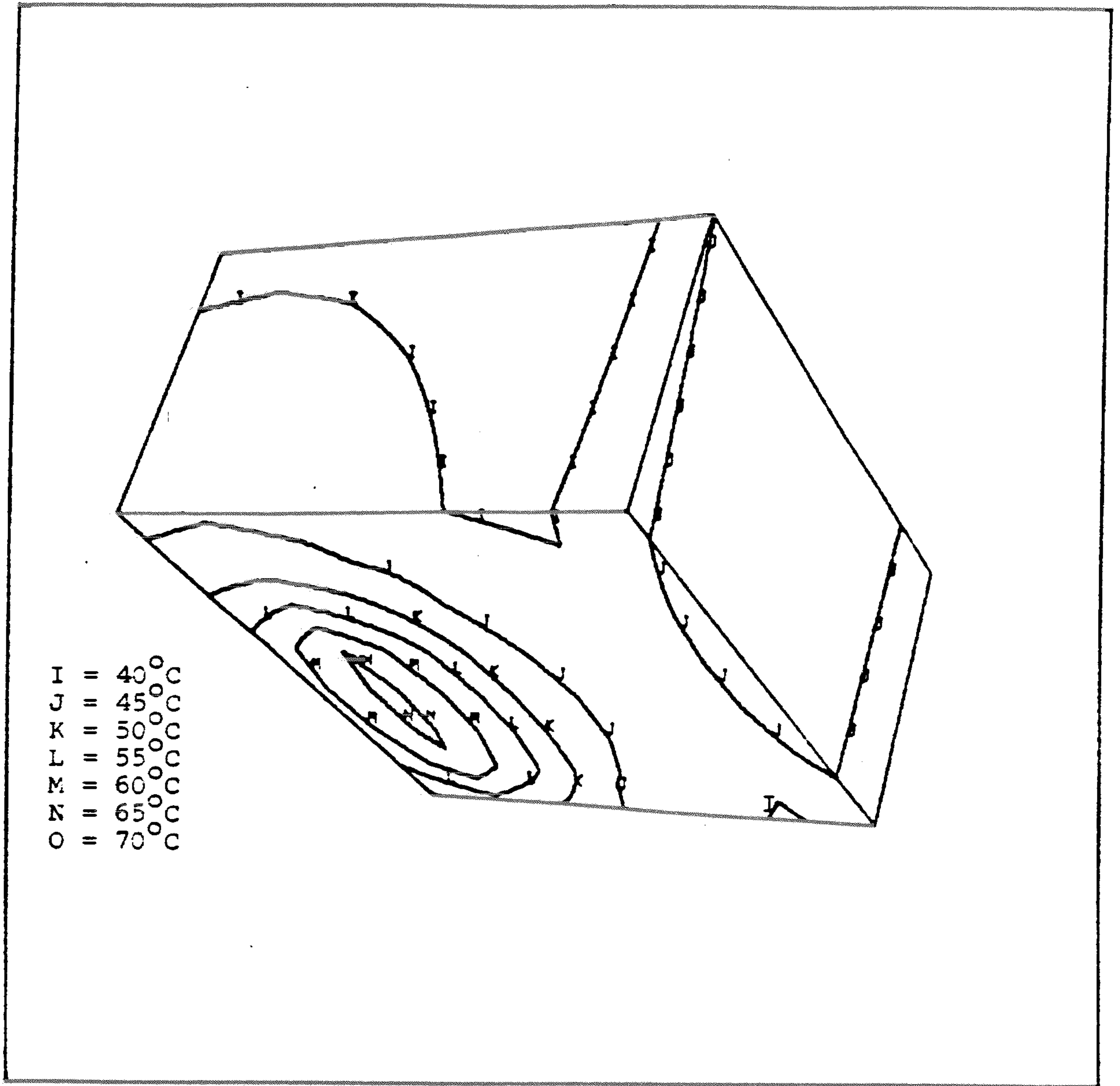


FIGURE 13