ENGINEERING SYSTEMS

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MSC/NASTRAN Transient Thermal and Thermal Stress Analysis of a Surface-Mounted Chip Capacitor

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ABSTRACT

Two recent MSC/NASTRAN Users' Conference papers (1,2)* discussed steady-state thermal analysis of surface mounted chips in automotive ignition systems. This paper applies MSC/NASTRAN transient thermal (SOL 89) and thermal stress (SOL 61) analyses to surface mounted chips. Possible temperature gradients and/or thermal stress due to thermal expansion coefficient mismatch in the assembly are investigated. Results are summarized graphically to evaluate design iterations.

INTRODUCTION

Surface mounted electronic components result in inexpensive fabrication, miniturization, and high speed performance. However, fabrication temperature cycling and operational power cycling often cause thermal and/or mechanical stress failure. Recently a finite element analysis of a surface mounted capacitor was completed (3). In that investigation MSC/NASTRAN SOL 89 was used to predict surface mounted chip and printed wiring board (PWB) spatial and temporal temperature variation during a 165 C temperature cycling test. SOL 61 was next used to determine local octahedral shear in the several components during the same test.

Graphical (XY) plotting is used to show assembly cool down behavior, while color stress contours (and noncolor lines of constant stress as reported here) are used to show areas of high stress gradients.

PHYSICAL ARRANGEMENT

Figure 1 shows a barium titanate ceramic chip capacitor surface mounted to a copper pad attached to an epoxy-glass PWB. The figure shows solder wedges on either end deposited by a reflow soldering technique or wave soldering technique (3). The wave-solder configuration was used in this investigation.

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*See Reference section

A stagnant air volume between the lower chip surface and upper PWB surface contributes a conduction barrier (no convection). All outer surfaces shown in Figure 1 (chip top and edge, PWB bottom, and wave-solder exposed surface) are cooled by an assumed-constant convection heat transfer coefficient to a spatially uniform air temperature that decreases suddenly in a cool down cycle.

FINITE ELEMENT MODELS

Figure 2a shows a solid element model of the chip capacitor assembly components using MSC/NASTRAN HEXA and PENTA elements. A quarter symmetry model was used with adiabatic boundary conditions (thermal analysis) and symmetric boundary conditions (stress analysis) on the two planes of geometric symmetry. Appropriate thermal properties (see Table 1) were supplied on MAT4 cards or mechanical properties on MAT1 cards for the thermal and thermal stress analyses, respectively. These values came from a literature search (3).

Figure 2b shows surface convection elements (CHBDY) for the thermal analysis only. Spatially uniform convection coefficients and ambient temperature are assumed.

Data recovery was obtained at GRIDs and solid element centroids for the thermal and thermal stress analysis, respectively.

TRANSIENT THERMAL ANALYSIS

Biot Modulus

It may be easily shown (4) that many transient heat flow problems have negligible internal thermal resistance compared to surface (convection) thermal resistance. If the Biot modulus (B=hL/k, see Table 1 nomenclature) is less than 0.1, temperatures throughout the cooled body will vary spatially by less than 5 per cent during a transient thermal process.

Table 1 shows L and B for each chip capacitor assembly component convectively cooled with a uniform convection coefficient of 0.0095

W/sq in °C. Hence, this convection coefficient will show negligible spatial temperature variation within the assembly during cool down for all components exposed to ambient air.

Solution Technique

A SOL 89 analysis was performed with the entire chip-capacitor assembly initially (IC) at 125°C. A common SPOINT to all CHBDY elements was maintained at -40°C for 840 seconds. A variable time step (2.5 second minimum, 60 second maximum) was used with the shorter time step implemented during the rapid initial cool down period.

The unknown uniform surface convection heat transfer coefficient was determined by adjusting this value until a close match to an experimental cool down curve was achieved.

Thermal Results

Figure 3 summarizes transient thermal results. The figure shows that a uniform surface convection coefficient of 0.0095 W/sq in °C nearly matches experimental cool-down measurements. Thus, the Biot moduli (see Table 1) were based on this value.

As expected all GRIDs showed identical temporal temperature variation during cool down.

THERMAL STRESS ANALYSIS

Solution Technique

Based on transient thermal results above, the Figure 2a finite element model was assigned Table 1 mechanical properties and a reference temperature (MAT1) of 125°C. A SOL 61 thermal stress analysis assigned each GRID -40°C temperature (TEMPD). Hence, each component showed an equivalent uniaxial thermal stress of $\sigma = -165*E*\alpha$ (see Table 1 nomenclature).

Thermal Stress Results

Octahedral shear stress was recovered at each solid element centroid (see Figure 2a). This stress was divided by an octahedral yield stress defined as 0.471 times uniaxial tensile yield stress for each material (3,5). These yield stress criteria and stress ratio ranges for the applied thermal load are tabulated in Table 2. The table shows that the solder has areas nearly three times yield, whereas the PWB has negligible stress.

Figure 4 shows areas of highest octahedral stress in the chip and in the solder nearest the copper pad. Both of these areas have shown failure in experimental investigations. However, a refined mesh may reduce these highly concentrated stress levels.

CONCLUSIONS

MSC/NASTRAN solutions 89 and 61 have proven successful in prediction of surface mounted chip assembly cool down and thermal stress, respectively. Future analyses would probably benefit from refined meshes (compared to those reported herein) for maximum thermal stress prediction, but the current mesh is more than adequate to predict temperatures in this 'lumped-parameter' approach to transient thermal analysis (Biot modulus less than 0.1).

Variation in component thermal expansion coefficients (within limits of physical reality) could be used to moderate thermal stress concentration.

Finally, the extremely high octahedral shear stress to octahedral shear yield stress ratios in the solder near the copper pad area suggest a SOL 66 (material nonlinear analysis) in future investigations.

REFERENCES

1. Cotner,J., et al, 'Finite Element Analysis of Darlington Transistor Stack', MSC/NASTRAN Users' Conference Proceedings, March 22 - 23, 1984.

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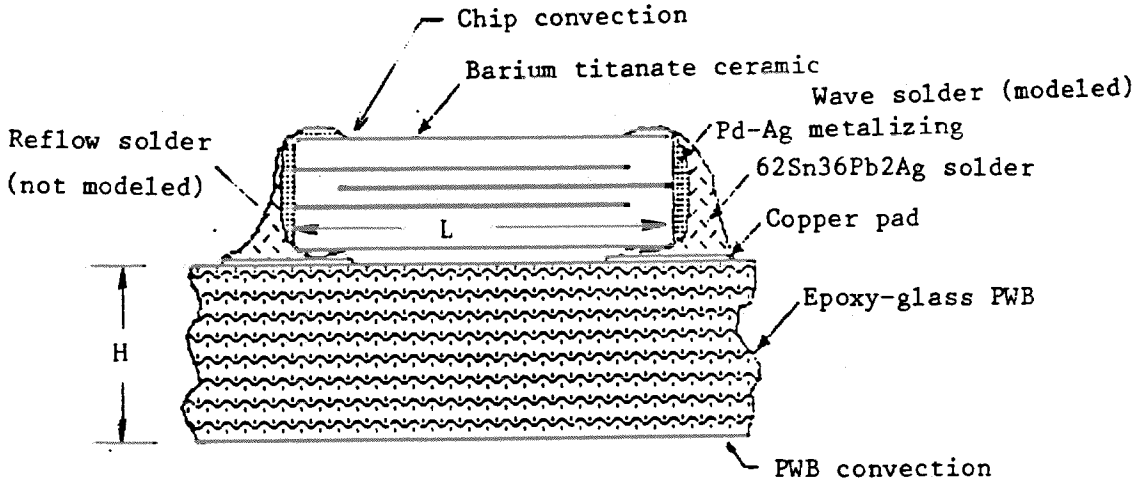
3. Epping, E. L., 'Thermal and Stress Analysis of a Surface Mounted Chip Capacitor Assembly Using the Finite Element Technique' MS-Engineering Thesis, University of Wisconsin - Milwaukee, WI, December, 1985.

4. Kreith, F., 'Principles of Heat Transfer', Third Edition, INTEX Press, New York, Chapter 4, 1973.

5. Boresi, A. P., et al, 'Advanced Mechanics of Materials', Third Edition, John Wiley and Sons, New York, 1978, p 121.



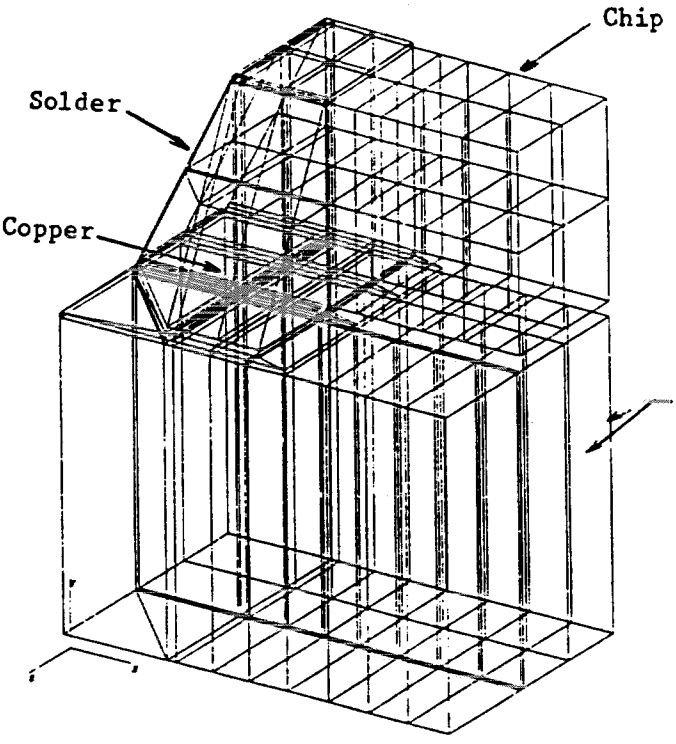
Chip cap = .125"L X .060"W X .040"H

Copper pads extend .025" beyond and .025" under each end of chip

Copper pads are .001" thick

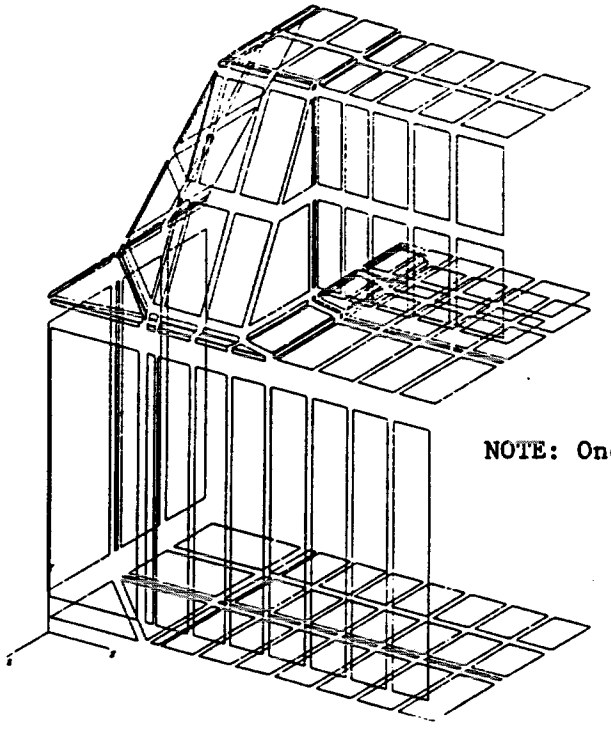
NOTE: PWB (full model) =
0.175"L X 0.11"W X 0.062"H

FIGURE 1. Chip Capacitor Assembly (Cross Section)



GRIDs : 287
HEXA : 146
PENTA : 18

a. Solid elements

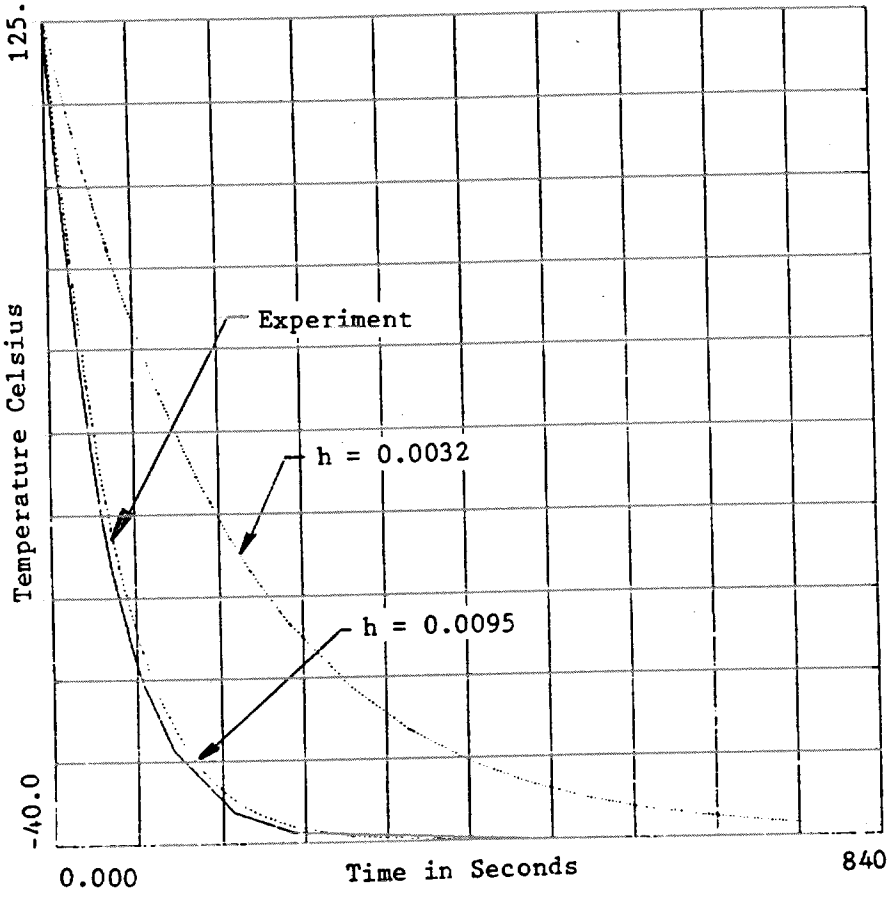


HBDY : 174

NOTE: One ambient air SPOINT used.

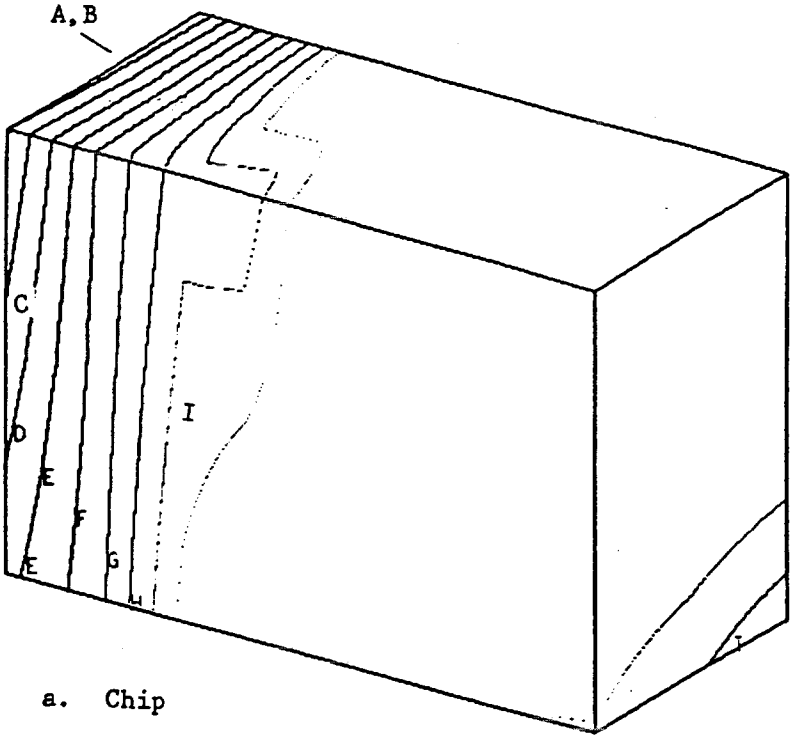
b. Surface convection elements (thermal analysis only)

FIGURE 2. Chip assembly Finite Element Model



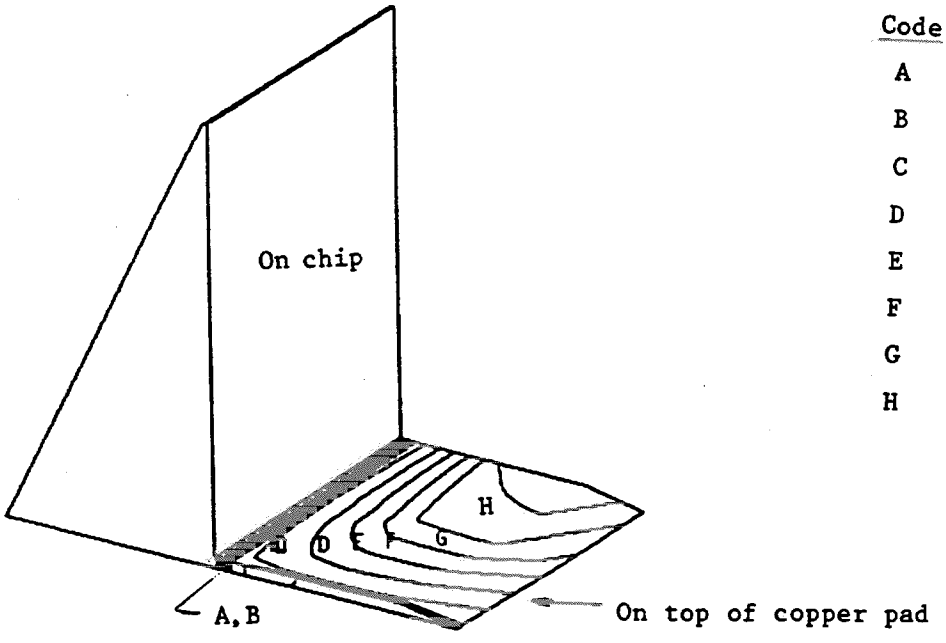
NOTE: All GRIDs same temperature at each time step.

FIGURE 3. Transient Thermal Results



a. Chip

Code	(psi)
A	2936
B	2754
C	2573
D	2391
E	2210
F	2028
G	1847
H	1665
I	1483



b. Solder

Code	(psi)
A	5092
B	4774
C	4457
D	4140
E	3822
F	3505
G	3187
H	2870

FIGURE 4. Thermal Stress Results, Octahedral Shear

TABLE 1. MATERIAL PHYSICAL, MECHANICAL, AND THERMAL PROPERTIES

	Physical Properties			Mechanical Properties			Thermal Properties			
Material*	A	V	L	E	ν	α	k	ρC	h	B**
Chip, Ba-Ti	175.	3.	0.017	10.00	0.22	7.00	0.1060	52.09	0.0095	0.002
Metalizing, Pd-Ag	--	--	--	12.00	0.30	27.25	8.5852	42.69	--	--
Epoxy, PWB	255.	12.	0.047	0.45	0.36	18.30	0.0043	31.51	0.0095	0.1
Copper	--	--	--	17.00	0.36	16.50	10.1092	56.50	--	--
Solder	34.	0.3	0.009	1.16	0.40	26.00	1.5940	28.36	0.0095	0.0
Air	--	--	--	--	--	--	0.0006	--	--	--

*See Figure 1.

**Biot modulus applicable to material cooled by convection.

Nomenclature: A - Convection surface area (10^{-4} in^2); V=volume (10^{-4} in^3); L=V/A

E = Elastic modulus (10^6 psi); ν = Poissons ratio
α = Coefficient of thermal expansion (μ in/in)

k = Thermal conductivity (watts/in °C); ρC = Thermal capacity (J/in^3 °C)
h = Convection coefficient (watts/in^2 °C); B = hL/k

TABLE 2.

MATERIAL YIELD STRESS, OCTAHEDRAL SHEAR AND STRESS RANGE

Material*	σy**	σoy**	$\sigma o/\sigma oy$
Chip, Ba Ti	6369	3000	0.314 - 1.008
Solder	6701	3156	0.67 - 2.858
Epoxy, PWB	10501	4946	0.042 - 0.046

*See Figure 1

Nomenclature: σy = Uniaxial yield stress (Psi)
σoy = Yield octahedral shear (0.471*σy)
$\sigma o/\sigma oy$ = Thermally-induced octahedral shears to yield octahedral shear ratio.

**See References 3 and 5.