FINITE ELEMENTS AND STRUCTURAL MECHANICS IN ELECTRONIC PACKAGING: PRESENT AND FUTURE

Arturo O. Cifuentes Ph.D.

IBM-East Fishkill
Hopewell Junction, NY 12533

ABSTRACT

This paper is concerned with the application of the finite element method to solve structural problems in electronic packaging. The paper presents an overview of some of the most common stress-related problems encountered in packaging, as well as their treatment using finite elements. A discussion regarding the use of commercial finite element codes in this environment is also presented.

INTRODUCTION

Electronic packaging (EP) is the art and science of designing and manufacturing the interconnections -- and the operating environment -- of the electronic circuits used to store and process information in computers.

This rather new discipline (only four books have been written on this subject [1-4], three of them after 1985), is one of the most challenging computer-related technical fields. This is mainly due to two factors: first, the fact that most EP problems involve several traditional engineering disciplines -- such as ceramic, chemical, mechanical, industrial, electrical and metallurgical engineering; and second, the increasing complexity of the new packages.

Until recently, most of the R & D efforts in EP were carried out by the industry, while the academic community remained indifferent to this field. This situation, however, has started to change. Another sign of the maturity of this field was the appearance in 1989 of the Journal of Electronic Packaging, published by the American Society of Mechanical Engineers. This is the first journal completely devoted to this field. Previously, most papers dealing with electronic packaging were scattered among other engineering publications such as IEEE Transactions, IBM Journal of R & D, Microelectronic Reliability, Solid State Technology, etc. In addition, since 1980, an international EP conference is held every year.

Some of the most interesting problems in EP today are stress-related problems. A number of these fall within the area of expertise of civil and mechanical engineers. However, most attempts to deal with these problems come from electrical engineers, applied physicists, etc. Moreover, the finite element method (FEM), which has been successfully used in civil and mechanical engineering, has only recently emerged as a design tool in EP. Its full power has not yet been exploited.

The goal of this paper is to: first, outline the typical stress problems encountered in EP; and second, discuss their treatment using state-of-the-art commercial FE codes. Some of these problems can be treated very accurately with the available codes while others call for capabilities not yet implemented -- at least in production codes.

DESCRIPTION OF A TYPICAL PACKAGE

The organization and structure of a package depends largely on the type of computer considered, the technology used, the material and processes involved, etc; therefore, it is difficult to discuss a typical package. Figure 1 is an attempt to represent a design which more or less captures the essential ingredients of the type of package used in mainframe systems.*

A summary description of the most important elements in this package is as follows (see Figure 1):

1) silicon chip;

2) solder joints (connect the chip to the substrate);

3) substrate (square plate-like structure usually made of ceramic);

4) pins (connect the substrate to the next packaging level); and

5) organic board.

Figure 1 does not intend to give a detailed description of all the elements involved in a typical package. It is simply a reference framework to discuss some structural mechanics problems.

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* A more detailed description of some typical packages can be found in Reference [1].

SOME TYPICAL STRUCTURAL PROBLEMS

This section presents a few structural mechanics problems that are currently of great interest to the EP community.

Pin Analysis

Consider Figure 2, which shows a pin connected to a substrate. This is a more detailed view of the pin structure depicted in Figure 1.

An important design consideration is the stress level at the substrate-pin interface. If these stresses are high they might damage the substrate. In principle, there are two unknowns in this problem: the forces acting at the tip of the pin, and the stress field at the substrate-pin interface.

First, the maximum loads acting at the tip of the pin should be calculated. This can be done simply by modeling the whole substrate-pins-board assemblage with a FE model. The board behaves like a plate and can be modeled using an array of regular plate elements. The same holds for the substrate. The pins can be modeled with two or four beam elements each. Then, the model is subjected to a variety of loading conditions representing the operating and testing environment. An analysis of this type has been described by Kelly et al. [5].

The second step consists in taking the maximum values observed for the forces at the tip of the pin and performing a detailed FE analysis of an individual pin (Figure 2). This will determine the stresses at the substrate-pin interface. (Notice the similarity between this problem and a typical pile design problem encountered in soil mechanics.)

Strictly speaking, this second step calls for a three-dimensional analysis using solid elements, or a two-dimensional analysis using axisymmetric elements subjected to axisymmetric and non-axisymmetric loads. However, to date, no such study has been reported in the literature. Most studies deal with this problem using a two-dimensional plane stress or plane strain model [5, 6]. This is largely due to the fact that most people in the EP community are familiar with simple two-dimensional FE programs developed in-house. In addition, the fact that the few commercial codes that can handle non-axisymmetric loads with axisymmetric elements are not yet user friendly has contributed to this situation.

A more complicated version of this problem, namely, the assumption that the solder obeys a nonlinear stress-strain law, is beyond the scope of most codes offering axisymmetric analysis capabilities.

Solder Joint Analysis

Figure 3 shows a detailed view of a typical solder joint that connects the chip and the substrate. The silicon chip has a thermal expansion coefficient which could be one half or one third that of the substrate. During its lifetime, this structure is generally subjected to a large number of 'thermal cycles', that is, a sequence of temperature oscillations that vary, roughly, between ambient value and 100 degrees Celsius. Consequently, chip and substrate do not deform uniformly and significant residual stresses are built up in the solder joints. These stresses need to be quantified accurately to predict the performance of the joint during the lifetime of the product.

This problem has been studied analytically using some fairly simplistic two-dimensional models in which linear behavior is assumed; only shear deformations at the solder joints are taken into account, and both chip and substrate are modeled as beams [7-10].

More elaborate analyses using FE have been reported in the literature [11-13]. In general these analyses consider a plane strain model, material properties constant with temperature, and small strains.

However, the actual chip-substrate assembly is more complicate. First of all, the problem is really three-dimensional. Second, the solder joint is in a complex strain state which can be fully described only in terms of shear, bending, and axial deformations rather than shear alone. In addition, the stress-strain relationship of the solder joint -- which is not totally understood to date -- is cumbersome. It exhibits hysteretic behavior and temperature dependent material constants. All these factors should be taken into account in a realistic FE model to make valid predictions. Finally, the load on the chip due to the heat sinks (not shown in the figure), can produce a creep phenomenon.

It is clear that an analysis incorporating all these features, and possibly large strains in the solder behavior, is beyond the range of capabilities of most commercial codes. However, a two-dimensional analysis, taking into account plastic behavior and considering temperature dependent material properties would be -- at least for same cases -- a reasonable compromise. Such analysis could be undertaken with current commercial codes, although no results have yet been reported in the literature.

This problem will continue to challenge the EP industry, since an important design consideration is the avoidance of crack-related failures in the solder joints.

Cracks in Organic Boards

The organic board shown in Figure 1, although it behaves as a homogeneous plate under certain conditions, is really a composite. The general structure of this

composite, which can consist of several layers of epoxy-glass laminates, is described in Figure 4. The thin copper layers are for power and signal transmission.

The vertical perforation depicted in the figure in known as a plated-through hole. The internal surface of this perforation is covered with a thin layer of copper, typically known as "barrel plating". An important design consideration is to avoid copper cracking in the vicinity of the plated-through holes since this can open a circuit and produce a failure.

As in the previous example, a major cause of crack development is the residual stress accumulated during operation. This occurs as a result of the thermal expansion coefficient mismatch between the copper and the epoxy-glass.

Some FE studies of this problem have been reported [14, 15], but there is still much room for improvement. Most studies consist of two-dimensional linear models in which the thermal expansion coefficient of the epoxy-glass is assumed to be constant. Actually, this coefficient is different in the X, Y, and Z direction. Moreover, in the Z direction it is also a function of the temperature. In addition, copper exhibits some plastic deformation before cracking which might require a nonlinear analysis.

This problem will keep receiving attention in the future since the influence of several factors in the crack formation process needs to be better understood. Among these factors are: barrel plating thickness, filler material composition, hole aspect ratio, and the presence of voids between laminates.

Other Problems

Among other problems, whose treatment using FE still leaves room for significant contributions, are the following: dynamic analysis of packages during testing and operation, chip fracture due to residual stresses, substrate failure due to high stresses at supports, crack propagation in connections due to residual stresses.

USE OF COMMERCIAL FINITE ELEMENTS CODES IN ELECTRONIC PACKAGING ANALYSIS

The use of FE techniques in EP has only recently started to become popular. A significant number of studies have been done using rather simple in-house codes. The major codes used in the aerospace and automotive industries (MSC/NASTRAN, ABAQUS, ANSYS) have had limited usage in EP, although this situation is expected to change.

At this moment, none of the major commercial FE codes is able to satisfy all the demands of the EP industry. This should not discourage potential users, since the power of the commercial codes has not yet been fully explored. In fact, in spite of their present limitations, the range of problems they can handle is very broad.

Ideally, a commercial FE code suitable for EP analysis should include the following features (in addition to the well known conventional linear and nonlinear capabilities):

a) Large displacement analysis including a large strain formulation,

b) Nonlinear axisymmetric elements,

c) User-friendly interface to define non-axisymmetric loads on axisymmetric elements,

d) Hysteretic material behavior combined with temperature dependent material constants,

e) Temperature dependent thermal expansion coefficients for all three directions,

f) Creep laws able to resemble the behavior of solder joints,

g) Crack propagation in two- and three-dimensional problems including isotropic and orthotropic behavior,

h) Shape optimization.

CONCLUDING REMARKS

The FE method, a technique that has reached a state of maturity in many engineering applications, has only recently emerged as a serious player in EP. As more civil and mechanical engineers get involved in EP, the use of FE will become widespread. Very interesting developments should be expected in the future.

In the sixties, the aerospace industry led many FE developments motivated by its own necessities. The same happened later on with the nuclear energy and automotive industries. It is expected that as new disciplines become more sophisticated they will make more demands on FE developers. In this regard, the EP industry, due to the growing demand for faster and smaller computers, will pose unique challenges to FE developers. It can be speculated that it will stimulate several advances in this field, especially in areas such as fracture mechanics, composite materials, more general stress-strain relationships, fatigue analysis and optimization.

Finally, it must be pointed out that structural problems are not the only type of EP problems amenable for FE analysis. The design of the cooling system in charge of dissipating the power generated by the chips presents many challenging questions to heat transfer analysts. Most of these cases can be studied using FE, although a detailed discussion of this subject is beyond the scope of this paper.

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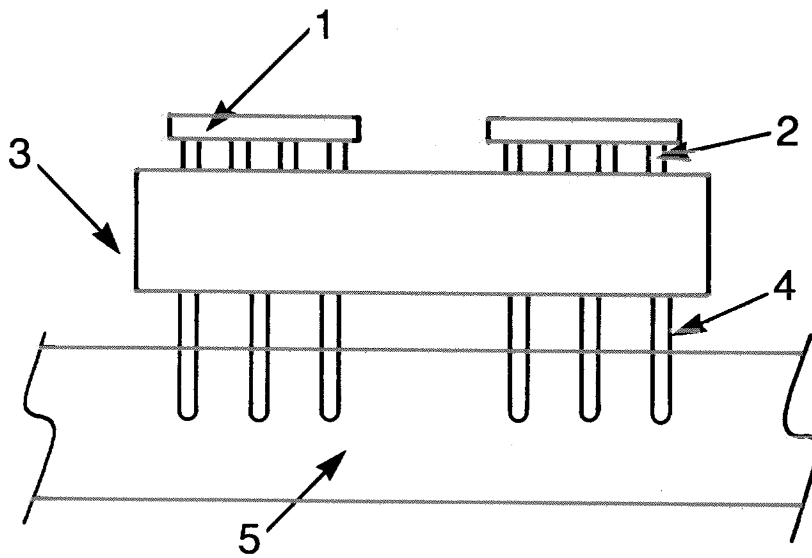

FIGURE 1. Main components of a typical package.

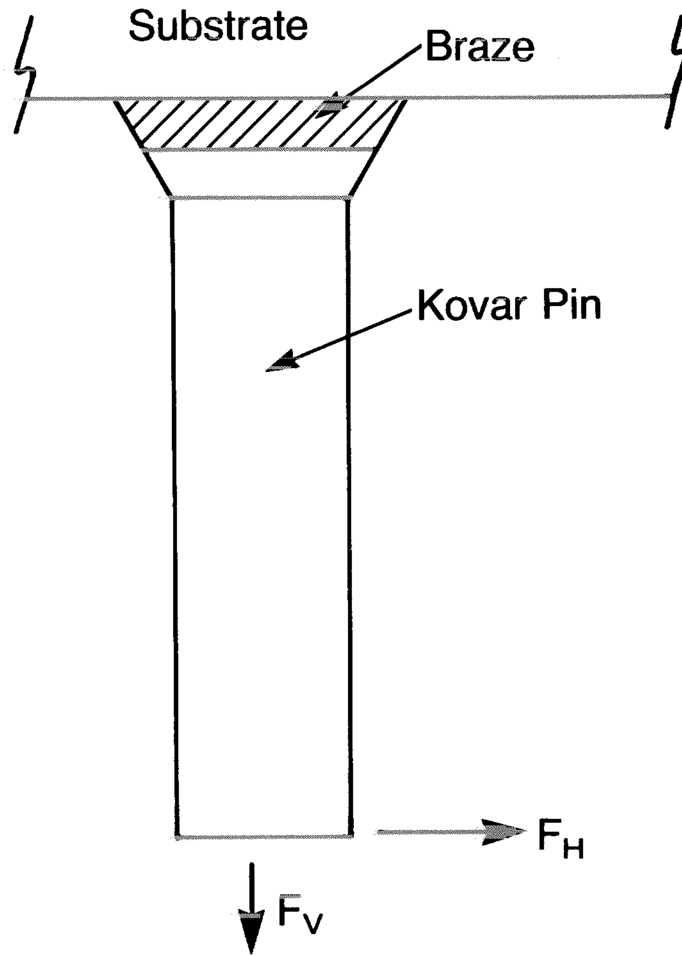

FIGURE 2. Pin.

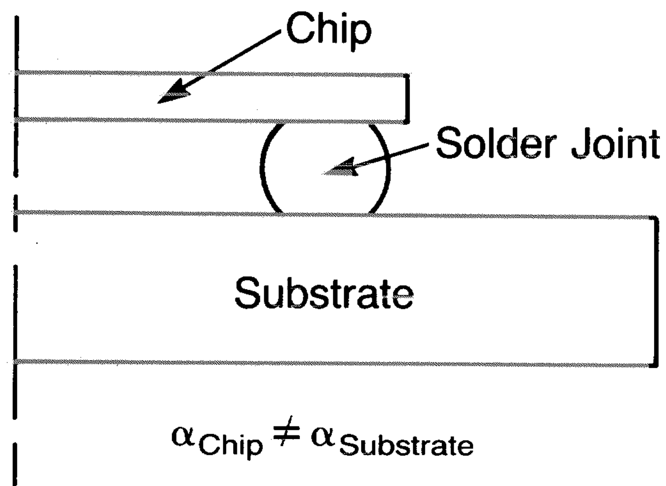

FIGURE 3. Detailed view of chip and substrate attachment.

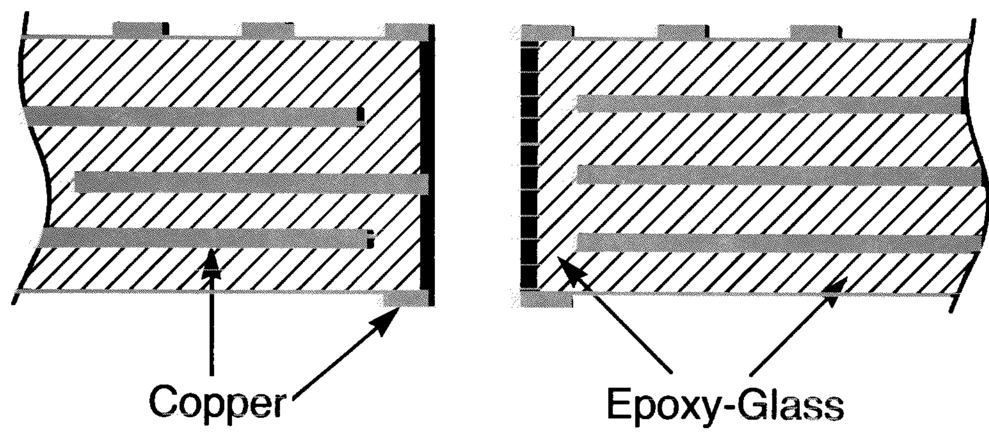

FIGURE 4. Cross section of organic board.