THERMAL DESIGN OF POWER MOSFETS OPERATING IN PARALLEL

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ABSTRACT

The objective of this paper is the thermal design analysis of power MOSFETs operating in parallel and which uses phase change immersion cooling. The heat generation (electrical power dissipation) in such devices is a function of the device resistance and the current through the device, both of which are functions of junction temperature of the device. The junction temperature, in turn, depends on the thermal resistance between the junction and the fluid which is a function of the boiling heat transfer coefficient, and the power dissipated. The analysis presented in this paper considers this complex interdependency in the design of heat sinks such that the temperature is below the limit required by reliability consideration. Thermal coupling of MOSFETs minimizes the junction temperature.

INTRODUCTION

Power MOSFETs are used in many electronics applications such as high speed switching devices and to perform other functions involving high power. They dissipate large values of power over a very small area resulting in very high heat flux and the thermal design of such devices becomes very critical. Thermal design for these FETs is very important because the failure rate of these devices is a function of junction temperature. Most specification require that junction temperature be kept below 110^{o} C or even lower to meet the system reliability requirements. The failure rate above this limit increases very rapidly. Conventional heat sink design for such devices will not be adequate to maintain the junction temperature below that required by reliability considerations. Immersion cooling with its inherent high heat transfer rates is required in such cases.

PROBLEM DEFINITION

The schematic diagram of power MOSFET is shown in Figure 1. It consists of a silicon die which is attached to a substrate with eutectic bond. The substrate is, in turn, attached to the base of a case by means of thermal bond. The hermetically sealed lid provides protection from the effects of ambient. In the present analysis, immersion cooling using Fluorinert (FC-72 from 3-M Inc.) is assumed. Fluorinert liquids are very inert, has very high dielectric strength, and acts as a good coolant. The boiling characteristics of FC-72 has been studied very extensively [Reference 1]. The high power involved in such devices, results in phase change (boiling) of the Fluorinert coolant. The electrical power dissipated in the silicon die is transferred to the case through the bonding layers and the substrate, from which it is ultimately transferred to the ambient fluid. In these devices, the electrical power dissipated P depends upon the electrical resistance of the device which is a function of the junction temperature T_j. Expressed mathematically the following expression results:

$$P = f(T_j) \tag{1}$$

The heat removal rate q in such devices is determined by the heat transfer coefficient h, the surface area A available for the heat removal, and the temperature differential between the case and the fluid saturation temperature ($T_w - T_s$). This can be expressed as follows:

$$q = hA(T_w - T_s) \tag{2}$$

The case temperature T_w is related to the junction temperature by the power dissipated, and the junction to case thermal resistance R_{jc} and is given as:

$$T_j = T_w + P\ R_{jc} \quad (3)$$

If the heat removal rate q does not balance the heat generation rate P, then the device temperature changes until equilibrium is reached. If the thermal capacity of the device is C the equation governing the temperature change is given by the following expression:

$$C\ dT_w / dt = P(T_j) - q(T_j) \quad (4)$$

Stable operation of the device requires that the heat removal rate balance the heat generation rate. Stable operation of the device can be shown in Figure 3. In this figure, the bold line curve represents the heat generation rate given by equation 1. This figure also shows the curve of heat removal rate for equilibrium conditions (dotted line) derived from equations 2 and 3. For equilibrium the two curves must intersect. In case the two do not intersect as depicted by the upper curve (jagged), operation of the device will cause an increase of junction temperature which will increase the power dissipated which will further increase the junction temperature. The device will eventually burn up due to thermal runaway. If equilibrium can be achieved, the operating junction temperature is shown by the intersection of the two curves. In case the two do not intersect, heat sink will have to be designed such that not only the two curves intersect but also at a point such that the junction temperature of the device is below what is required by the system reliability requirements. In many applications, the junction temperature limits are very stringent. The present analysis considers the heat generation (power dissipation) mechanism first, which may be termed as the electrical characteristics, followed by heat removal mechanism from the device which may be termed the thermal characteristics.

ANALYSIS

Electrical Characteristics

Electrical power dissipation in a MOSFET can occur due to various effects [Reference 2]; they are a) Switching Transition Loss P_S ; b) Power dissipated in the gate structure P_G ; c)Power loss due to drain to source leak P_L ; d) the reverse diode conduction loss P_D ;
e) Conduction loss while the device is on P_C. The first four losses are small and independent of the junction temperature. Their sum can be represented as a constant P_0. The major loss is due to non-zero resistance $R_{DS(on)}$ through which the drain to source current must flow. The loss can be expressed as:

$$P_C = (I_{DS})^2 R_{DS} \quad (5)$$

The total power dissipation is therefore represented by the following:

$$P = P_0 + P_C \tag{6}$$

The first term in the above equation represents the constant part, and the second varying part of the total power dissipation. The drain to source resistance R_{DS} (subscript DS will be omitted for brevity) increases with junction temperature and vendors provide the curve of this resistance as a function of junction resistance as a function of junction temperature T_j. When MOSFETs operate in parallel, the current through the individual MOSFETs I_1 and I_2 are given in terms of the individual resistances R_1 and R_2 by Ohm's law as follows:

$$I_1 = IR_2 / (R_1 + R_2); \qquad I_2 = IR_1 / (R_1 + R_2) \tag{7}$$

In the above expression a constant total current I is assumed. The individual resistances R_1 and R_2 are functions of the respective junction temperatures T_j and can be expressed as follows:

$$R = R_0 \, f(T_j) \tag{8}$$

R_0 is the nominal resistance at 25° C and the multiplier function $f(T_j)$ is normally provided by vendors in the form of a curve (Figure 2). The power dissipation in the individual MOSFETs P_1 and P_2 are now given by the following:

$$P_1 = (IR_2 / (R_1 + R_2))^2 \, R_1 \tag{8}$$

$$P_1 = (IR_1 / (R_1 + R_2))^2 \, R_2 \tag{9}$$

R_1 and R_2 are given by the functional relationship similar to equation 4. From the above expressions 3-9, it can be seen that as junction temperature increases, the device resistance increases and the current shared decreases. Thus an increase in power dissipation will cause an increase in of junction temperature which will lower the resulting current and the power. Operation of the device in parallel has the inherent property of self regulation. It will not result in thermal runaway, which is a characteristics of the device when operated alone. In a similar manner, thermal coupling will further result in lower operating temperatures.

Thermal Characteristics

When the device is turned on, power is dissipated in the silicon junction (given by equation 5) which is transferred to the fluid via the substrate and the case. If the heat generation exceeds the heat removed, the junction temperature increases, the rate being determined by the thermal capacity of the device. At equilibrium, the heat generated is exactly balanced by the heat removal rate. In the early part of the transient, where the surface temperature of the transient where the surface temperature of the device below the fluid boiling point, the heat transfer mechanism is by natural convection and is given by the well known correlation between the Nusselt Number NUS, Grashoff Number Gr, and the Prandtl Number PR [Reference 3] as follows:

$$NUS = 0.333\ GR^{0.333}\ PR^{0.8} \tag{10}$$

In the natural convection regime, the heat generated by the device is well in excess of the heat removed resulting in an increase of case temperature. As the surface temperature increases, vapor cavities begin to form and ultimately nucleate boiling sets in. The correlation for fully developed nucleate boiling is given by the Roshenow's correlation [Reference 1] as follows:

$$C_p\ (T_w - T_s) = C_{sf}\ (q/\mu_l\ i_{lg}\ [g_c\sigma / g(\rho_l - \rho_g)]^{0.6})^{0.33}\ PR^{1.7} \tag{11}$$

C_p is the specific heat of the liquid, T_w is the case temperature, T_s is the fluid saturation temperature, i_{lg} is the latent heat of vaporization, C_{sf} is an empirical constant, q is the heat flux, μ is the viscosity of the fluid, σ is the surface tension, ρ_l and ρ_g are the liquid and vapor densities respectively. PR is the Prandtl Number. Transition regimes between natural convection and fully developed nucleate boiling regimes were not modeled in detail. A simple interpolation between the two regimes were used.

Thermal Modeling

Thermal analysis was performed using the finite element code PATRAN/PTHERMAL from MacNeal-Schwendler Corp. In the analysis the silicon die, the substrate, and the case were represented by shell elements. Contact resistances were included at various interfaces to give the correct vendor supplied junction to case resistances. The heat transfer regimes, the current shared by the devices, the resistances of the individual devices, and the power dissipated by the devices were incorporated in the user supplied subroutines, a very powerful feature of PATRAN/PTHERMAL software. For the

purposes of the present analysis, the resistances of the individual devices were assumed to be 0.2 and 0.4 watts respectively. Power input was in the form of uniform volumetric heat source over the silicon die. The mismatch in the resistance between the two MOSFETs will produce uneven heating and different junction temperatures. A total of 7 amps was assumed for the circuit current. A total of 2400 finite element nodes were created in the analysis. Transient runs were made starting from an ambient temperature of 50^{o} C, the maximum expected ambient temperature for operation.

DISCUSSION OF RESULTS

Figure 3 shows the plot of junction temperatures of the MOSFETs without any thermal coupling. It is seen from the plot that the difference the two temperatures is large as much as 12^{o} C when steady state conditions are reached. MOSFET1 has higher junction temperature because of its higher electrical resistance and more power dissipation. Figure 4 shows the plot of junction temperature when the two MOSFETs are thermally coupled by connecting them with a heat sink as shown in Figure 1. Because heat flows from the hotter MOSFET1 to the cooler MOSFET2, the difference between the junction temperature of the device is now less than when they were thermally uncoupled. Reduction of temperature difference also improves the load sharing since the difference between the two device resistance is less. It is seen from the plot that the junction temperature of the MOSFET1 is now 118^{o} C still higher than the desired 110^{o} C. Figure 5 shows the attachment of heat sinks to individual MOSFETs in addition to the thermal coupling heat sink. The resulting temperature profile is shown in Figure 6 from which it is seen that the junction temperature is below the desired goal of 110^{o} C.

CONCLUSIONS

Operation of power MOSFETs in parallel will prevent thermal runaway. In addition, thermal coupling will decrease the junction temperature difference between the device. Care must be exercised while selecting heat sinks and their attachment.

ACKNOWLEDGMENTS

The author wishes to acknowledge the user support group of MacNeal-Schwendler Corporation for the help provided in the write up of the user supplied subroutines.

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1. Bergles , “Boiling Heat Transfer”, Hemisphere Publishing Co., 1981
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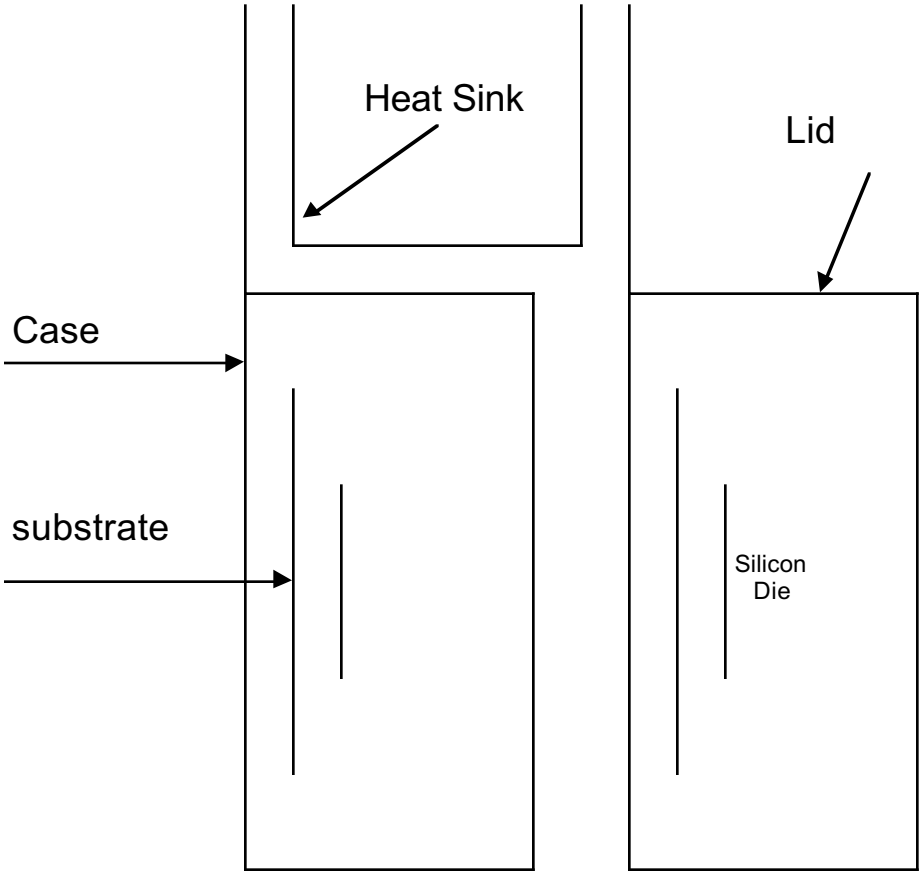

Figure 1 Schematic Diagram of Power MOSFETs Operating in Parallel

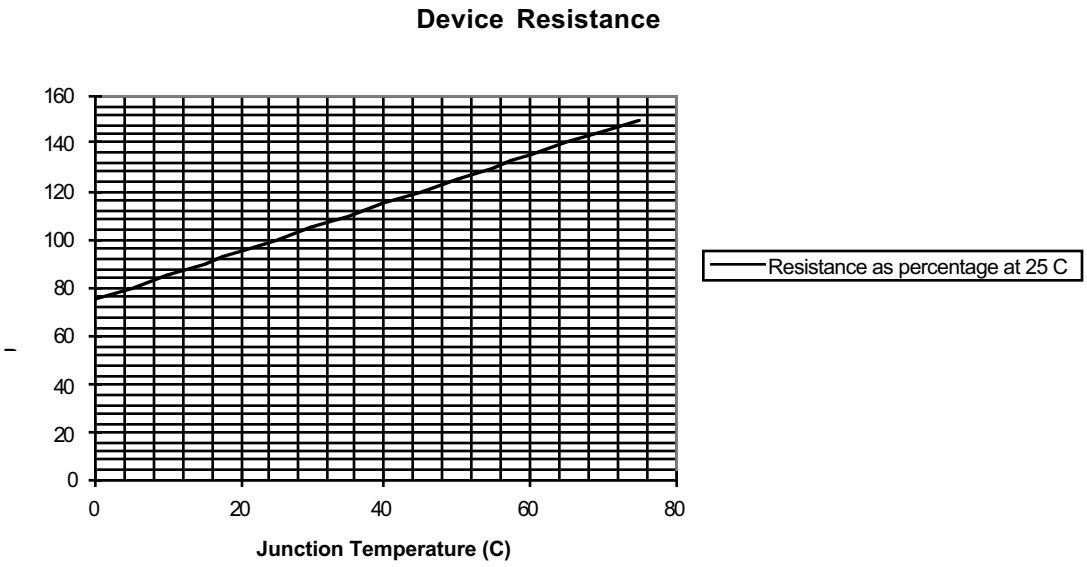

Figure 2 Device Resistance

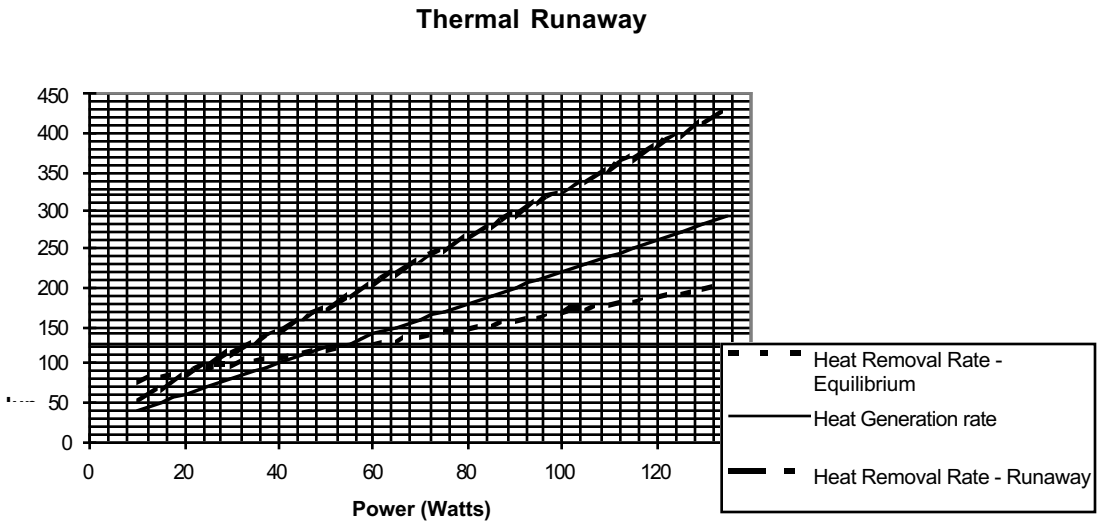

Figure 3 Graphical Determination of Thermal Runaway

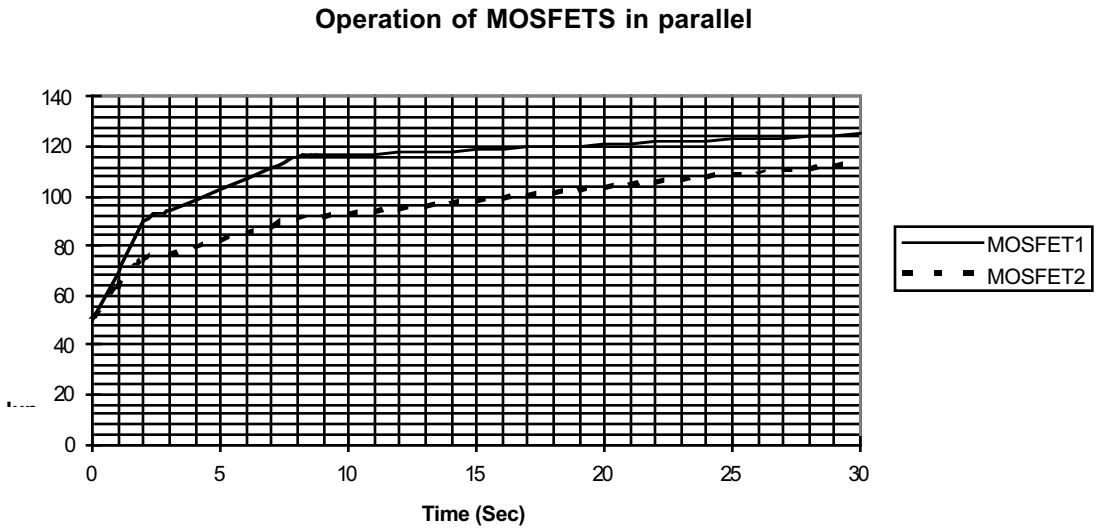

Figure 4 Operation of MOSFETs without Thermal Coupling

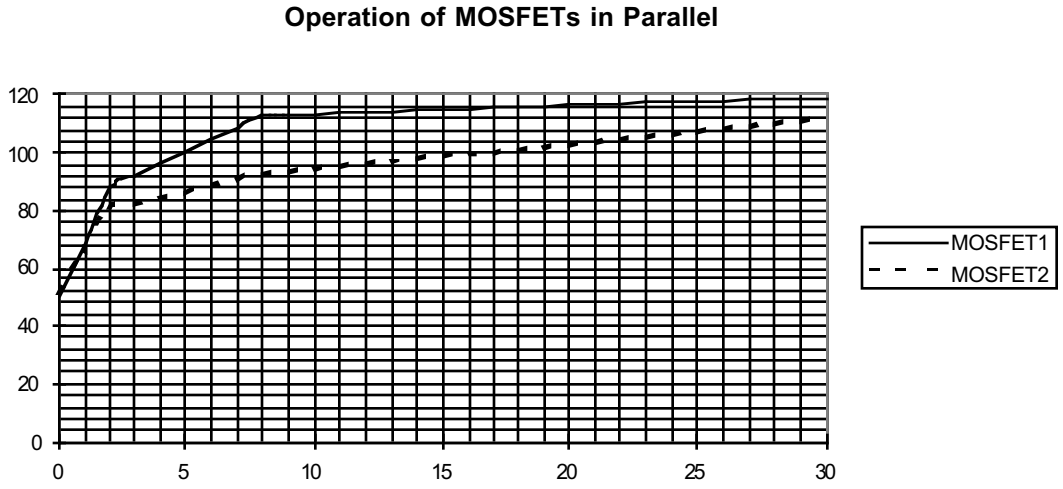

Figure 5 Operation of MOSFETs with Thermal Coupling

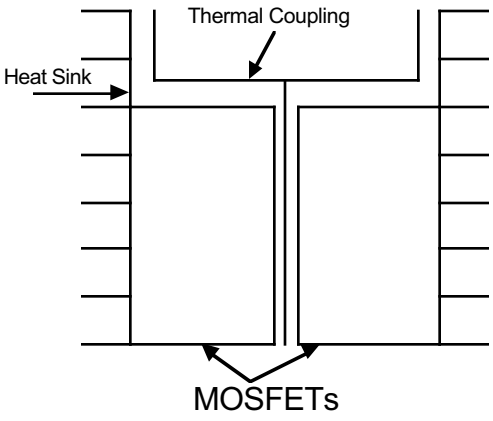

Figure 6 MOSFETs with Thermal Coupling and Finned Heat Sinks

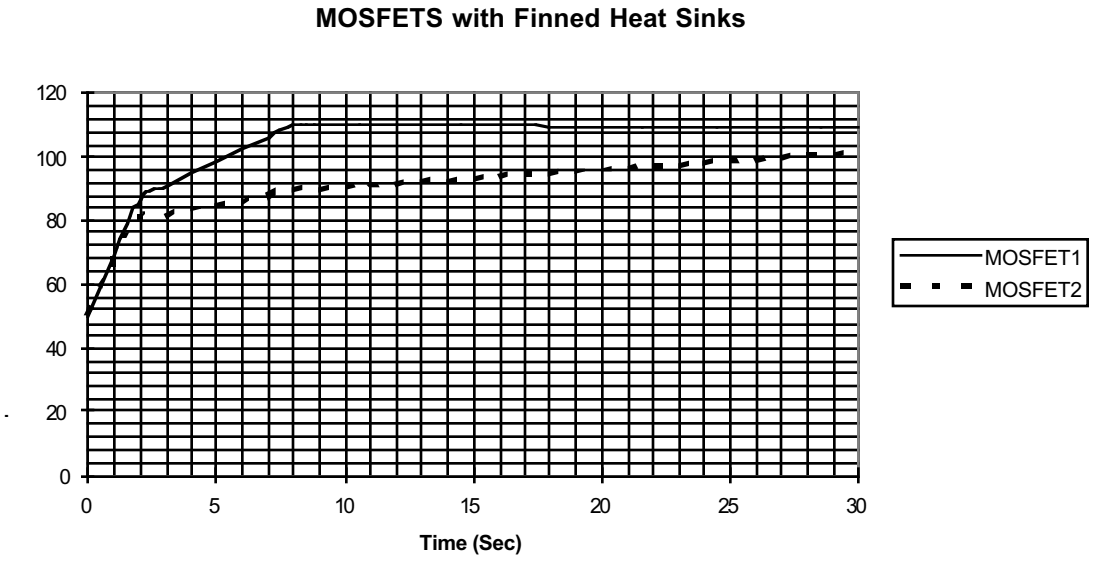

Figure 7 Operation of MOSFETs with Finned Heat Sinks